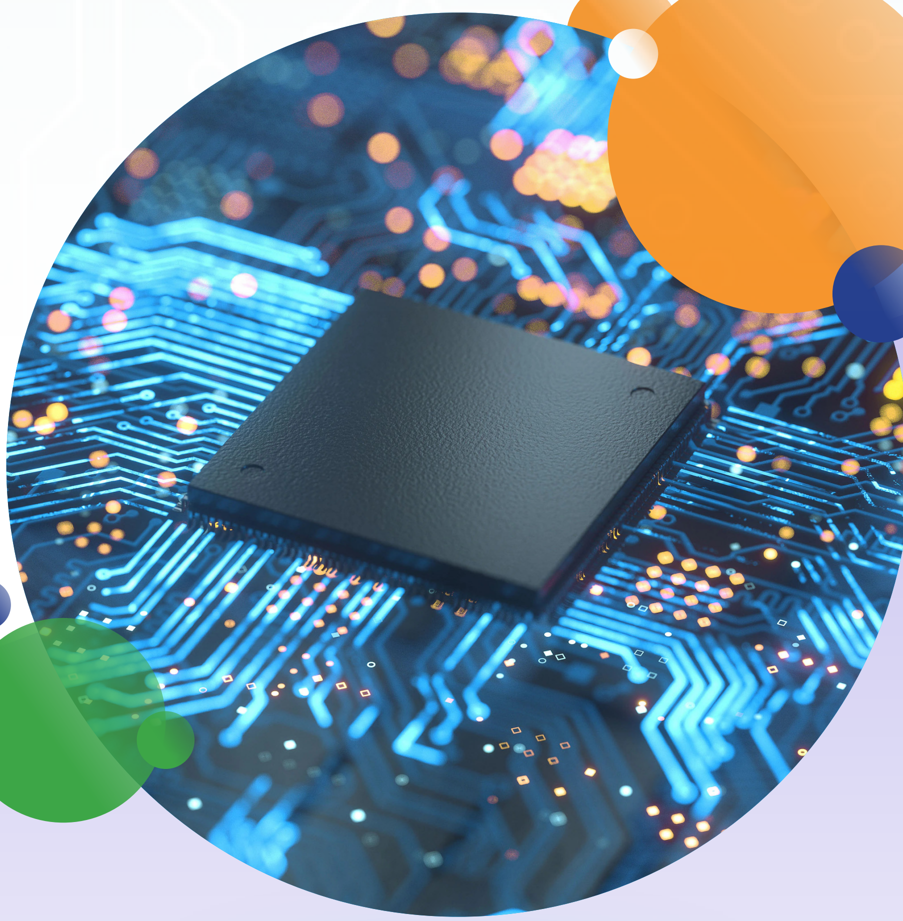
Report of Workshop on Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities



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Strengthening India's Semiconductor Ecosystem Policies, Challenges, and Opportunities

Organized under the Project

Comparative Analysis of Global Semiconductor Policies and Strategies vis-à-vis India's Semiconductor Ecosystem

(CSPS24/RDSF/NIScPR/IHP25/02)

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Proceedings of the Workshop on "Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities" at CSIR-NIScPR, New Delhi, 27 February 2026.

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The workshop on "Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities," was held on 27 February 2026 at CSIR-National Institute of Science Communication and Policy Research (CSIR-NIScPR), New Delhi.

We extend our sincere gratitude to Dr. Geetha Vani Rayasam, Director, CSIR-NIScPR, for her constant encouragement, visionary leadership, and institutional support in organizing this workshop. We also express our sincere thanks to Prof. V. Ramgopal Rao, Group Vice-Chancellor, BITS Pilani, for gracing the workshop as the Chief Guest and delivering an inspiring address.

We also extend our sincere appreciation to all the distinguished speakers and experts from academia, government, R&D institutions, and industry whose active engagement enriched the workshop discussions, including NITI Aayog, SSPL-DRDO, IISc Bangalore, Research and Information System for Developing Countries (RIS), BITS Pilani, IIT Delhi, IIT Jodhpur, Delhi Technological University, Amrita University, CSIR-CEERI, CSIR-CSIO, CSIR-NPL, and CSIR-NAL. We are also grateful for the participation of industry leaders from global and domestic semiconductor organizations such as Intel, Lam Research (Semiverse Solutions), Applied Materials, AMD, Sahasra Semiconductor Private Limited, and VerveSemi Microelectronics Pvt. Ltd for their insights.

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We hope that the insights and deliberations captured in this will contribute to actionable policy recommendations, foster stronger collaborations among stakeholders, and help chart a clear roadmap toward technological self-reliance and global competitiveness in India's semiconductor sector.

Authors

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Executive Summary

The CSIR-National Institute of Science Communication and Policy Research (CSIR-NIScPR) organized a one-day workshop titled "Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities" on 27 February 2026 at Pusa Campus, New Delhi. The workshop brought together experts from government, academia, industry, and research institutions to deliberate on key issues shaping India's semiconductor ecosystem. It was conducted in support of a CSIR-NIScPR study examining global semiconductor policies in comparison with India's approach.

The primary objective of the workshop was to assess India's current semiconductor landscape, identify major challenges, explore opportunities for growth, and generate actionable policy recommendations. The event saw participation from around 100 attendees in person and over 200 participants online, representing institutions such as MeitY, NITI Aayog, IITs, IISc, CSIR laboratories, and leading semiconductor companies.

The inaugural session emphasized the importance of evidence-based policymaking and sustained stakeholder engagement. A key issue highlighted was India's "semiconductor paradox," where the country has strong capabilities in chip design but remains heavily dependent on imports. Speakers stressed the need for innovation-driven policies, strategic investments, and a long-term vision to establish India as a global semiconductor hub.

The workshop featured three thematic sessions. The session focused on R&D, design, and manufacturing, and experts highlighted the need to strengthen India's semiconductor value chain through investment in pilot fabrication facilities, promotion of indigenous materials and equipment, and encouragement of design-led innovation. Emerging areas such as photonics, artificial intelligence-based chips, and sustainable manufacturing ecosystem for semiconductor were identified as key growth domains. The session also emphasized the importance of intellectual property generation and international collaboration.

In the session on workforce and skill development, experts emphasized on the urgent need to bridge the skill gap in semiconductor manufacturing and design. Strengthening academic programs, introducing industry-relevant curricula, and promoting structured training initiatives were identified as critical steps. Greater collaboration between academia and industry was seen as essential for building a skilled workforce and supporting long-term growth.

On policy, governance, and institutional frameworks, discussions highlighted the need for a coordinated policy approach and stronger institutional mechanisms. Experts emphasized on learning from global best practices, improving access to critical raw materials, enhancing supply chain resilience, and promoting semiconductor diplomacy to reduce external dependencies.

The experts in panel discussion emphasized on the strategic pathways for India's semiconductor future. Panelists acknowledged progress made under government initiatives such as the India Semiconductor Mission but stressed the importance of effective implementation, innovation, and scaling. They highlighted the need for advanced manufacturing capabilities, specialized talent, and stronger partnerships between industry and academia. Emerging technologies such as chip architectures and quantum-integrated systems were identified as potential areas for future leadership.

The workshop also identified key challenges, including high capital requirements, limited access to advanced technologies, supply chain vulnerabilities, and gaps in translating research into commercial outcomes. Addressing these challenges will require sustained investment, policy support, and coordinated efforts across stakeholders.

Several recommendations emerged from the discussions. These included establishing a National Semiconductor Authority and a National Semiconductor Research Center, promoting shared research infrastructure and pilot fabrication facilities, strengthening industry-academia collaboration, establishment of National Technology Hub, and enhancing global partnerships. Experts also emphasized focusing on niche areas such as compound semiconductors, sensors, and photonics.

Overall, the workshop underscored the strategic importance of semiconductors for economic growth, technological advancement, and national security. It highlighted the need for integrated efforts across policy, research, manufacturing, and skill development to enhance India's position in the global semiconductor value chain.

Background of the workshop

The global semiconductor industry stands at the forefront of technological transformation, powering innovations in artificial intelligence, 5G and beyond, electric mobility, quantum technologies, and advanced manufacturing. Recognized globally as a strategic asset, semiconductors now underpin economic competitiveness, national security, and technological sovereignty. In response, leading nations are advancing policies to build resilient, self-reliant, and innovation-driven semiconductor ecosystems. India has made significant efforts in positioning itself within this global value chain. Key initiatives such as the India Semiconductor Mission (ISM), Production-Linked Incentive (PLI) schemes for semiconductor and display manufacturing, and the Design-Linked Incentive (DLI) program reflect the country's strategic commitment to developing a vibrant domestic ecosystem encompassing design, manufacturing, and research.

CSIR-NIScPR, as a national institute dedicated to science policy research and science communication, plays a critical role in supporting India's vision through evidence-based policy research. The institute's expertise in S&T policy analysis, technology foresight, innovation studies, and stakeholder engagement makes it uniquely positioned to facilitate multi-sectoral dialogue.

CSIR-NIScPR has undertaken research to study the Comparative Analysis of Global Semiconductor Policies and Strategies vis-à-vis India's Semiconductor Ecosystem'. This workshop was organized to achieve the objectives of the project.

This interactive workshop aims to bring together R&D institutions, policymakers, academia, and industry leaders to deliberate on critical challenges and opportunities shaping India's semiconductor future. Discussions will focus on assessing India's current policy landscape, benchmarking it against global leaders, identifying systemic gaps, and formulating strategies to foster innovation, investment, and global competitiveness.

Expected Outcomes

- Actionable policy recommendations to strengthen India's semiconductor ecosystem
- Identification of priority areas for strategic interventions
- Insights from global best practices and their applicability to India
- A roadmap for fostering collaboration among government, industry, and academia toward technological self-reliance

Inaugural Session

Prof. V. Ramgopal Rao (Chief Guest), Group Vice-Chancellor, BITS Pilani, Dr, Geetha Vani Rayasam, Director, CSIR-NIScPR, Dr. Vipan Kumar, Chief Scientist, CSIR-NIScPR, Dr. Naresh Kumar, Chief Scientist, CSIR-NIScPR and Dr. Shiv Narayan Nishad, Principal Scientist, CSIR-NIScPR, New Delhi

Welcome Address: Dr. Geetha Vani Rayasam, Director, CSIR-NIScPR

Dr. Geetha Vani Rayasam, Director of the CSIR-National Institute of Science Communication and Policy Research, welcomed participants from government, academia, industry, and CSIR laboratories, and introduced the institute's activities. She highlighted that CSIR-NIScPR was established in 2021 through the merger of National Institute of Science Technology and Development Studies and National Institute of Science Communication and Information Resources to integrate science communication with policy research.

Dr. Rayasam also contextualized the workshop within an ongoing comparative study of global semiconductor ecosystems, covering countries such as the United States, Taiwan, South Korea, Japan, and China. She underscored the importance of adapting global best practices to India's context while maintaining international standards. The workshop, she noted, marks an important step toward developing evidence-based policy recommendations for policy makers and decision makers to strengthen India's semiconductor ecosystem.

Conceptual Framework & Setting the Context of Workshop: Dr. Vipan Kumar, Chief Scientist, CSIR-NIScPR

Dr. Vipan Kumar, Chief Scientist CSIR-NIScPR, outlined the conceptual framework and rationale for the workshop by emphasizing the strategic importance of semiconductors. He began with an anecdote from his aerospace experience, where a restriction on a critical semiconductor component disrupted an indigenous project, illustrating India's technological vulnerability. He further highlighted the global semiconductor shortage during COVID-19 pandemic, which caused massive economic losses and significantly impacted industries such as automobiles in India.

Dr. Kumar pointed out India's heavy reliance on imports, meeting nearly 95% of its semiconductor demand externally, despite contributing about 20% of the global design workforce, yet it remains overwhelmingly dependent on imported chips, termed the "India Semiconductor Paradox." He outlined the government's response through the India Semiconductor Mission (ISM) 1.0 and positioned the workshop as a bridge toward a more innovation-driven ISM 2.0. The CSIR 2030 Policy, targeting semiconductor chip development and high-technology self-sufficiency, was cited as the institutional framework guiding CSIR's own contribution.

Concluding, he outlined the study's methodology, triple-helix (industry-academia-policy) engagement model, including global case studies and stakeholder engagement, and identified key focus areas: gap analysis, niche technology prioritization, talent development, and leveraging geopolitical opportunities like the "China+One" strategy.

Main Highlights of the Presentation

- Highlighted strategic importance of semiconductors for national security and economic growth
- Shared aerospace example showing technology vulnerability due to import dependence
- Referenced COVID-19 semiconductor shortage and its impact on industries like automobiles
- Identified ~95% import dependency despite strong domestic design capabilities
- Explained the "India Semiconductor Paradox" (high design talent, low manufacturing capacity)
- Linked efforts to CSIR 2030 Policy for self-reliance in semiconductor technology
- Identified focus areas: gap analysis, niche technologies, talent development, and China+One opportunities

Chief Guest Address: Prof. V. Ram Gopal Rao, Group Vice Chancellor, BITS Pilani

Prof. V. Ram Gopal Rao delivered a comprehensive keynote address on India's semiconductor strategy, emphasizing the need to move beyond macroeconomics of semiconductor manufacturing to the structural barriers impeding India's transition from a talent-rich nation to a product-innovation powerhouse. Using the "Smile Curve" concept, he illustrated that in any product value chain, the highest value-add increases at the conceptualization/design end and the marketing/sales end, while manufacturing occupies the lowest value-add position unless it strengthens product conceptualization and intellectual property (IP) generation. He cautioned that merely establishing semiconductor fabrication plants in India without simultaneously building an indigenous product conceptualization ecosystem would replicate the Foxconn model rather than the Apple model. Using Apple and Foxconn model as a case study, he noted that Apple which performs no manufacturing, is valued at approximately USD 3-4 trillion, while Foxconn, which manufactures for Apple, is valued at approximately USD 60-70 billion.

Professor Rao observed that while India has over 120 unicorn companies, less than 5% of the country's unicorns, are based on intellectual property or patents. He argued that most Indian unicorns are based on business-model innovations that can be easily replicated, rather than on deep-technology innovations that offer stronger protection. He called for fostering deep-tech startups and creating a "Flipkart of Deep Tech" to catalyze an innovation-driven ecosystem. He noted that Indian unicorns have predominantly been built by undergraduate alumni (B. Tech. graduates) rather than PhD researchers with deep domain expertise, reflecting a structural deficit in research-to-product translation pathways. Stressing the importance of patient capital for frontier science and long-term R&D investment, he argued for stronger collaboration between academia, industry, and national missions to anchor the fundamental research, and IP-based companies.

Prof. Rao supported investments in 28 nm semiconductor technology, which is adequate for approximately 80% of applications and is the most accessible technology on the global market. But advocated diversification into high-potential areas such as sensors fabs, flex photonics fabs, power electronics, solar PV fabrication, discrete power and RF devices (gallium nitride, silicon carbide), packaging fabs, and automotive-grade analog ICs. He was particularly enthusiastic about the sensors market, noting that industry projections point to a potential trillion-sensor-per-year market, representing a trillion-dollar opportunity even at a per-unit price of USD 1.

Prof. Rao presented a "7P Framework" (Problem, Project, Patents, Papers, Prototypes, Products, Profits) for deep tech startup creation. Prof. Rao emphasized that 95% of Indian academic research currently terminates at papers and patents, never progressing to prototypes or products. He argued that individual faculty members cannot be expected to bridge this 'valley of death' alone; institutional mechanisms like National Semiconductor Translation Hubs are required to take technologies from TRL 3 to TRL 8. He suggested that CSIR laboratories could and should occupy this bridging role between academia and industry. Prof. Rao presented the good example of successful translation of technology like NanoSniffer - a micro-sensor-based explosive detector developed at IIT Bombay and NPK Soil Sensor, which has demonstrated a 27% reduction in water usage, 40% reduction in chemical inputs, and benefited over 25,000 farmers across 40,000 hectares. He argued that individual faculty members cannot be expected to bridge this 'valley of death' alone; institutional mechanisms like National Semiconductor Translation Hubs are required to take technologies from TRL 3 to TRL 8. He called for ISM 2.0 to pose grand challenges - analogous to ISRO's satellite launch targets or DRDO's missile programmes that would focus India's academic and research talent on specific national problems solvable through semiconductor and sensor technologies. He also highlighted importance of R&D budget spent in India and China, which spends more on two universities (Tsinghua and Peking) than India's entire MHRD budget, underscoring the scale of India's R&D investment deficit. He concluded by urging large-scale R&D investments and mission-driven innovation to position India as a global technology leader.

Main Highlights of the Presentation:

- Emphasized shift from manufacturing focus to building a product-innovation ecosystem for semiconductors
- "Smile Curve" concept illustrated that in any product value chain, the highest value-add increases at the conceptualization/design end and the marketing/sales end, while manufacturing occupies the lowest value-add position unless it strengthens product conceptualization and intellectual property (IP) generation
- Stressing the importance of patient capital for frontier science and long-term R&D investment in semiconductor sector
- Warned against replicating the Foxconn model; advocated for an Apple-like innovation-driven approach
- Identified low deep-tech penetration (<5%) among India's 120+ unicorns as a major gap
- Called for nurturing IP-driven deep-tech startups and a "Flipkart of Deep Tech"
- Highlighted weak research-to-product translation, especially lack of PhD-led innovation
- Advocated diversification into high-potential areas such as sensors fabs, flex photonics fabs, power electronics, solar PV fabrication, discrete power and RF devices (gallium nitride, silicon carbide), packaging fabs, and automotive-grade analog ICs.
- Indian unicorns have predominantly been built by undergraduate alumni (B. Tech. graduates) rather than PhD researchers with deep domain expertise, reflecting a structural deficit in research-to-product translation pathways
- 7P Framework" (Problem, Project, Patents, Papers, Prototypes, Products, Profits) for deep tech startup creation and to guide lab-to-market technology translation
- Recommended for establishment of institutional mechanism 'National Semiconductor Translation Hubs' to bridge this 'valley of death' and to take technologies from TRL 3 to TRL 8 and to market
- Emphasized on focus of India's academic and research talent on specific national problems solvable through semiconductor and sensor technologies
- Advocated large-scale R&D investments and mission-driven innovation in the semiconductor sector to position India as a global technology leader

Open Discussion

Following the Chief Guest's address, discussions focused on CSIR's role, innovation challenges, and technology strategy. On CSIR, Professor Rao emphasized its ideal position as a bridge between academia and industry, aligning research capabilities with industrial needs. However, he noted a drift toward academic competition, stressing the need for policy changes to restore its bridging function. Discussing the 7P Framework through the Nano Sniffer case, he highlighted the long, iterative journey from research to commercialization. Early failures, funding struggles, and restrictive procurement policies delayed progress, with significant breakthroughs only after 2021 and large-scale deployment by 2025. He stressed that innovation is slow and policy-dependent.

On semiconductor investments, concerns about 28-nanometer technology becoming obsolete were addressed by noting its relevance for most applications. Rao argued that pursuing advanced nodes is impractical due to high costs and limited technology access, advocating instead for indigenous product development.

Key Takeaways

- **The India Semiconductor Paradox*:*** India remains highly dependent on semiconductor imports (~95%) despite strong global design capabilities (~20% globally), highlighting the "India Semiconductor Paradox."
- **Weak Research-to-Product Translation Mechanisms**: Research ends at papers/patents; limited lab to land technology transfer and commercialization ("valley of death").
- **Creating Enabling Institutional Mechanisms for Research-to-Product Translation**: Establish translation hubs using the 7P framework to bridge lab-to-market gaps, and creation of institutional mechanisms such as **National Semiconductor Translation Hubs** that can support the transition of technologies from laboratory research (TRL 3) to advanced prototype and pre-commercial stages (TRL 8).
- **Promoting Deep-Tech and IP-Driven Entrepreneurship**: Few startups based on core technology; reliance on business-model innovation. Need pf promoting Deep-Tech and Intellectual Property–Driven Startups through funding, incubation, and policy support.
- **Gaps in Academia–Industry–Research Collaboration**: Weak linkages hinder technology transfer and innovation scaling.
- **Constraints in Manufacturing and Technology Access**: High costs, tech barriers, and risk of obsolescence.
- **Funding and Long-Term Investment Challenges**: Lack of patient capital for deep-tech development.
- **Talent Development and Curriculum Alignment**: Skill gaps in specialized semiconductor training.
- **Regulatory and Procurement Barriers**: Strict norms delay startup adoption and scaling.
- **Insufficient R&D Investment:** Broader challenge of limited national investment in research and development compared to leading technological economies. Sustained progress in semiconductor

technologies requires substantial and continuous investment in advanced research infrastructure, university laboratories, and industry partnerships.

- **Prioritizing Product Innovation alongside Semiconductor Manufacturing**: Focus on design, IP, and product ecosystems, not just fabrication, to capture higher value.
- **Supporting Patient Capital for Frontier Technology Development & R&D**: Enable Supporting patient capital mechanisms, through public funding, institutional support, and long-horizon investment frameworks for advancing deep-technology innovation and strengthening India's semiconductor ecosystem, and sustained investment in fundamental research, prototype development, testing, and product validation for successful science translation requires over extended time horizons
- **Adopting a Diversified Semiconductor Manufacturing Strategy**: Expand beyond fabs into sensors, photonics based devices, power electronics based on gallium nitride and silicon carbide, solar photovoltaic technologies, semiconductor packaging, and automotive-grade analog integrated circuits.
- **Strengthening the Semiconductor Sensor Ecosystem**: Invest in sensor technologies and fabrication capabilities as a strategic growth area with wide applications and high global market potential.
- **Introducing Mission-Oriented National Technology Challenges**: Launch targeted national missions to align research with strategic needs, focus on areas, including advanced sensors, semiconductor devices for strategic applications, and next-generation electronics systems.
- **Strengthening the Role of National Research Institutions**: Position labs as bridges between academia and industry for faster commercialization by understanding industrial requirements and supporting the development of prototypes and technology validation.
- **Strategic Way Forward: A** balanced approach is needed, prioritizing product innovation, strengthening deep-tech startups, enabling research translation, diversifying manufacturing into emerging areas, fostering mission-driven programmes, and empowering national institutions to bridge ecosystem gaps.

Session I: R&D and Innovation, Design and Manufacturing Ecosystem

Highlights of the Session

This session was chaired by Dr. Rajesh Kumar Sharma, Former Director, Solid State Physics Laboratory (SSPL), DRDO; Chairman, Semiconductor Society of India, and co-chaired by Dr. Naresh Kumar, Chief Scientist, CSIR-NIScPR, New Delhi

The first session focused on strengthening the research, innovation, design, and manufacturing ecosystem required to support the growth of India's semiconductor sector. The discussion emphasized the need for a coordinated approach that integrates academic research, industry participation, policy support, and manufacturing capability to build a resilient and competitive ecosystem aligned with national technological and economic goals.

Expert Talk 1: Strategic Niche Focus and Pilot Fabrication for Compound Semiconductors Dr. Manish Mathew, CSIR-CEERI, Pilani

Dr. Manish Mathew highlighted India's position remains absent or marginal across the semiconductor value chain, noting heavy dependence on imports for equipment and materials, while India contributes meaningfully to chip design, material quality for semiconductor-grade applications remains insufficient; and end-product assembly is the dominant domestic activity. He argued that competing in commodity segments is unviable due to global cost disadvantages, particularly against China. Instead, India should focus on niche, high-value, and strategically critical areas where technology is denied to India by foreign governments, where the application is strategically critical, or where the market commands a premium price, such as high-electron-mobility transistors (HEMTs), RF devices, MEMS sensors, and defense-related technologies where entry barriers and technology denial create opportunities.

A key recommendation was the establishment of pilot fabrication facilities, low-cost cleanrooms to produce limited volumes of high value compound semiconductors and bridge the gap from lab to pilot scale (TRL 3–7). Priority areas include GaN, silicon carbide power electronics, diamond semiconductors, multi-junction solar cells and MEMS sensors as priority focus areas. He also highlighted import substitution opportunities, especially in UAV solar cells. Dr. Mathew emphasized on shared national cleanroom facility, accessible to university researchers, national laboratories, and industry was proposed as a means to support the transition from TRL 3-4 (laboratory scale) to TRL 5-7 (pilot scale). Dr. Mathew highlighted a specific import substitution opportunity: unmanned aerial vehicles operated by NAL (National Aerospace Laboratories) require approximately 30 square meters of gallium arsenide multi-junction solar cells at a cost of approximately ₹20 crore per set, all of which is currently imported. He estimated this could be manufactured domestically using approximately 2,000 gallium arsenide wafers in a pilot fab.

The talk concluded with recommendations for regional semiconductor clusters across India, each focusing on a specific technology area; incentives for deep-tech fabless design in RF and power domains; seed funding mechanisms; and strengthened IP and commercialization pathways including mandatory patent filing as part of publicly funded research outputs.

Main Highlights of the Presentation:

- Highlighted India's weak position in semiconductor value chain with high import dependence for materials and equipment
- Noted strong design capabilities but limited manufacturing competitiveness
- Argued against competing in commodity segments due to cost disadvantages vs China
- Recommended focus on niche, high-value areas: HEMTs, RF devices, MEMS sensors, and defense technologies
- Proposed pilot fabrication facilities (low-cost cleanrooms) to bridge TRL 3–7 gap
- Identified priority technologies: GaN, silicon carbide, diamond semiconductors, multi-junction solar cells
- Highlighted import substitution opportunities, especially in UAV solar cells
- Suggested creation of regional semiconductor clusters with technology specialization
- Recommended incentives for deep-tech fabless design in RF and power electronics
- Emphasized seed funding, stronger IP frameworks, and mandatory patenting for publicly funded research

Expert Talk 2: Industry Perspective on Semiconductor Ecosystem Development - Ms. Deepakshi Mahendra, Government Affairs Lead, Intel India

Ms. Deepakshi Mahendra from Intel India presented an industry perspective on the evolving global semiconductor landscape and its implications for India. She emphasized that attracting global semiconductor companies requires strong and consistent domestic demand, both for components and end-use products, which has historically been a challenge in India.

She highlighted the need for policy coherence across the entire electronics value chain, from component manufacturing to system integration, to create a viable investment environment. Without aligned demand and policy support, local fabrication struggles to compete with globally optimized supply chains.

A key insight was that India's semiconductor strategy must prioritize integration into global supply chains rather than relying solely on import substitution. For long-term viability, semiconductor facilities must serve international markets. She concluded that future policy frameworks, particularly ISM 2.0, must align R&D, manufacturing incentives, and demand creation in a coordinated and integrated manner. She emphasized that Strong domestic demand, policy coherence, and global supply chain integration are essential to attract investment and ensure sustainable semiconductor manufacturing in India.

Main Highlights of the Presentation:

- Presented industry perspective on global semiconductor trends and India's position
- Emphasized need for strong and consistent domestic demand to attract global players
- Highlighted historical weakness in demand for components and end-use products
- Stressed importance of policy coherence across the value chain (manufacturing to system integration)
- Emphasized that semiconductor facilities must serve international markets for viability
- Called for coordinated policy approach in ISM 2.0
- Recommended alignment of R&D, manufacturing incentives, and demand creation
- Concluded that demand, policy coherence, and global integration are key to sustainable growth

Expert Talk 3: Academic Infrastructure and Skill Development for Semiconductors – Dr. Rahul Kumar, Associate Head, CREST, BITS Pilani

Dr. Rahul Kumar highlighted the expanding academic infrastructure and skill development initiatives in semiconductor technology at BITS Pilani. He described the Hyderabad campus cleanroom facility with Class 100 and Class 10,000 environments supporting full CMOS fabrication processes, along with plans to scale infrastructure at the Pilani and Goa campuses.

On the academic front, BITS Pilani has introduced specialized programmes, including a dedicated degree in Semiconductor and Quantum Systems, along with professional courses for industry practitioners. A key innovation is the "tape-out project," where students design and fabricate an indigenous chip, ensuring practical, outcome-based learning.

Dr. Kumar emphasized strong industry and global collaboration through joint research programmes, international academic partnerships, and startup incubation support. With funding and support from industry players, the center aims to evolve into a globally recognized semiconductor research hub that integrates education, research, innovation, and entrepreneurship.

Expert Talk 4: CSIR Photonics and Semiconductor R&D Initiatives - Dr. Umesh Kumar Tiwari, Senior Principal Scientist, CSIR-CSIO, Chandigarh

Dr. Umesh Kumar Tiwari presented CSIR's efforts in advancing semiconductor R&D with a strong focus on photonics-integrated systems and strategic sensor technologies. He highlighted that while India contributes over 20% of global chip design talent, its manufacturing and fabrication capabilities remain underdeveloped, underscoring the need for strengthening domestic infrastructure by investment in large scale to the domestic design and fabrication ecosystems across Bengaluru, Hyderabad, Chennai, Pune, and Uttar Pradesh like Taiwan Semiconductor Manufacturing Company (TSMC).

He noted that CSIR laboratories have historically operated in silos and emphasized the importance of aligning their work with national semiconductor priorities. CSIR-CSIO's key focus areas include miniaturized LEDs, optical gyroscopes, diffractive optical elements, micro/nano-optics, meta-surfaces, and quantum photonic integrated circuits, supported by advanced cleanroom facilities. CSIR-CSIO has recently established a world class photonics R&D facility with Class 1,000 and Class 10,000 cleanrooms, equipped with a direct laser writer, ICP etcher, and RF characterization tools.

Dr. Tiwari also highlighted emerging technologies such as augmented reality displays, photonic chips for data centers, terahertz antennas, biosensors, and quantum sensing. He stressed the importance of coordinated research efforts, sustained funding, and outcome-oriented R&D aimed at reducing imports, generating high-value jobs, and contributing to economic growth.

Main Highlights of the Presentation:

- Highlighted CSIR's focus on photonics-integrated systems and sensor technologies
- Noted India's strength in chip design (~20% global share) but weak fabrication capabilities
- Emphasized need for large-scale investment in domestic design and fabrication ecosystem
- Identified key hubs: Bengaluru, Hyderabad, Chennai, Pune, and Uttar Pradesh
- Outlined CSIR-CSIO focus areas: LEDs, optical gyroscopes, micro/nano-optics, meta-surfaces, quantum photonics
- Highlighted need of advanced cleanroom infrastructure facilities
- Showcased emerging technologies: AR displays, photonic chips, terahertz antennas, biosensors, quantum sensing
- Stressed need for coordinated research and sustained funding
- Emphasized outcome-driven R&D to reduce imports, create jobs, and boost economic growth

Expert Talk 5: Lessons from Semiconductor Infrastructure Development - Dr. Nirmalya Karar, Senior Principal Scientist, CSIR-NPL, New Delhi

Dr. Nirmalya Karar analyzed past semiconductor infrastructure efforts in India and drew lessons for future investments under the India Semiconductor Mission. He highlighted that institutions such as the Semiconductor Laboratory (SCL), DRDO's Solid State Physics Laboratory (SSPL), BITS Pilani, and GAETEC fulfilled their intended roles in research, specialized technology development, and talent creation rather than mass commercial production. These facilities contributed significantly to building India's foundational capabilities, particularly in sensors and compound semiconductors.

A key insight was the need to align infrastructure objectives with realistic economic and market conditions. Dr. Karar emphasized that semiconductor fabrication facilities have a limited operational life of about ten years, during which they must recover capital and operational costs. This requires a clearly defined product, market demand, competitive pricing, and efficient cost management. He stressed that future semiconductor investments must integrate technological capability with commercial viability to ensure long-term sustainability.

Expert Talk 6: Sustainable and Flexible Electronics: Emerging Directions for India - Prof. Shri Prakash Tiwari, Professor & Dean (Administration), IIT Jodhpur

Prof. Shri Prakash Tiwari presented sustainable and flexible electronics as a strategic opportunity for India to develop original research-to-product pathways. He noted that while India has made progress in semiconductor infrastructure, the broader ecosystem and effective intellectual property (IP) generation that translate into economic value remain underdeveloped. He highlighted emerging domains such as quantum computing, electronic skin for robotics and healthcare, neuromorphic computing, and electronic waste and sustainability as areas where India must act early to avoid missing future opportunities.

His research focuses on biodegradable and transient electronics enabled by additive manufacturing, which minimizes material waste compared to conventional subtractive methods. Demonstrations include biodegradable sensors, flexible electronic systems, and edible electronics using materials like rice. On neuromorphic computing, Professor Tiwari described hardware implementations of brain-inspired synaptic learning using flexible electronic devices, which offer the potential for low-power, high-speed computation at the device level. He argued that these emerging directions in biodegradable electronics, neuromorphic hardware, and electronic skin may represent areas where India could build global-first capabilities.

He concluded that achieving leadership in these areas requires an integrated approach combining education, R&D, innovation, and incubation within a cohesive semiconductor ecosystem.

Main Highlights of the Presentation

- Highlighted sustainable and flexible electronics as a strategic opportunity for India
- Noted gaps in ecosystem development and IP generation despite infrastructure progress
- Identified emerging areas: quantum computing, e-skin, neuromorphic computing, sustainable electronics
- Emphasized need for early action to capture future technology leadership
- Focused on biodegradable and transient electronics using additive manufacturing
- Highlighted benefits of additive methods (reduced material waste vs traditional processes)
- Showcased innovations: biodegradable sensors, flexible systems, edible electronics (e.g., rice-based)
- Discussed neuromorphic devices for low-power, brain-like computation
- Stressed importance of research-to-product pathways in new domains
- Concluded with need for integrated ecosystem combining education, R&D, innovation, and incubation

Open Discussion

The open discussion following the presentations was wide ranging and substantive, covering several interconnected themes.

The discussion explored key technical, institutional, and strategic issues in India's semiconductor ecosystem. On plasma technology, participants highlighted its potential in advanced packaging, especially for surface treatment and precision dicing of fragile MEMS devices. However, such processes are not yet industrially established in India, indicating a major R&D opportunity.

A debate on historical semiconductor facilities, the institutions like SCL and CSIR-CEERI have involved in technology development and workforce training. Their contributions underpin today's industry, and the focus should be on scaling and re-mandating them. On fabrication economics, it was noted that R&D fabs cannot sustain themselves through early revenues. Industry co-investment becomes critical at mid-TRL stages (5–7), requiring long-term commitment, as even large firms need years to validate indigenous chips.

India's limited progress in wide bandgap semiconductors (SiC, GaN) was attributed to fragmented research efforts lacking national alignment. A coordinated mandate could better utilize existing capabilities, as seen in missed opportunities like GaAs solar cells.

The session recommended that ISM 2.0 prioritize compound semiconductors and support indigenous equipment development, which requires long timelines. Finally, sensor commercialization challenges such as cross-sensitivity were discussed, with solutions involving multi-sensor arrays and advanced signal processing through collaborative research.

Closing Remarks

The session chair, Dr. Rajesh Kumar Sharma, offered closing remarks acknowledging the breadth and quality of the discussions. He observed that the session had surfaced both the significant latent capability within India's research institutions and the structural, economic, and organizational barriers that have historically prevented that capability from translating into commercial outcomes. He endorsed the recommendation for ISM 2.0 to focus on compound and wide bandgap semiconductors as a strategic priority.

Key Takeaways

- **Ecosystem Integration and Strategic Vision**
  The session emphasized that India's semiconductor growth depends on a **holistic ecosystem** integrating research, design, manufacturing, and policy support. A coordinated approach involving academia, industry, and government is essential to build a competitive and resilient semiconductor sector aligned with national priorities.
- **Need for Strategic Niche Focus**
  India cannot compete in mass-market semiconductor manufacturing dominated by global players. Instead, it should focus on high-value niche areas such as compound semiconductors, MEMS sensors, RF devices, and defense applications.
- **Establishing Pilot Fabrication Facilities for Advanced Materials and Devices**
  Strongly recommended the establishment of pilot-scale semiconductor fabrication facilities capable of producing limited quantities of high-value devices. These facilities would serve as a bridge between laboratory-scale research and commercial manufacturing by enabling technology maturation from early-stage research to pilot production levels
- **Importance of Market Demand and Global Integration**
  Sustainable semiconductor growth requires strong domestic demand and participation in global supply chains. Policies must ensure coherence across the entire value chain, from chip design to end-product manufacturing, rather than relying solely on import substitution
- **Strengthening Academic and Research Infrastructure**
  Institutions are expanding cleanroom facilities, specialized courses, and industry collaborations**.** Outcome-based learning approaches, such as chip tape-out projects, are crucial for developing practical skills and innovation capacity.

- **Role of CSIR and R&D Coordination**
  CSIR laboratories have strong capabilities in areas like photonics and sensors but need greater coordination and alignment with national semiconductor goals. Converging fragmented efforts can accelerate innovation and reduce import dependence
- **Lessons from Past Initiatives**
  Lessons from Semiconductor Infrastructure Development: Align fabs with market demand, defined products, and economic viability.
- **Emerging Technologies and Future Opportunities**
  New domains such as flexible electronics, biodegradable devices, neuromorphic computing, and quantum technologies present opportunities for India to build leadership if investments are made early. Emphasis on intellectual property creation is for start-ups recommended.
- **Need for National Focus Areas**: Prioritize wide bandgap semiconductors (GaN, SiC) through coordinated national mandates.
- **Key Challenges and Policy Directions**: Major challenges include import dependence, weak manufacturing infrastructure, and lack of institutional alignment. Policy recommendations include developing regional clusters, pilot fabs, support for wide bandgap semiconductors, and long-term R&D investment, along with stronger industry-academia collaboration.

List of Experts in the session

1. Dr. Rajesh Kumar Sharma, Former Director, Solid State Physics Laboratory (SSPL), DRDO; Chairman, Semiconductor Society of India-Chairman
2. Dr. Naresh Kumar, Chief Scientist, CSIR-NIScPR, New Delhi-Co-Chairman
3. Dr. Manish Mathew, Chief Scientist, CSIR-CEERI, Pilani
4. Ms. Deepakshi Mahendra, Government Affairs Lead, Intel India
5. Dr. Rahul Kumar, Associate Head of Centre of Research Excellence in Semiconductor Technologies, BITS Pilani
6. Dr. Umesh Kumar Tiwari, Senior Principal Scientist, CSIR-CSIO, Chandigarh
7. Dr. Nirmalya Karar, Senior Principal Scientist, CSIR-NPL, New Delhi
8. Prof. Shri Prakash Tiwari, Professor & Dean (Administration), IIT Jodhpur.

Session II: Ecosystem for Skill Workforce & Talent Development

Highlights of the session

This session was chaired by Dr. Manish K. Hooda, Director (Technology), India Semiconductor Mission (ISM), MeitY, New Delhi and Co-Chaired by Dr. Bornali Sarma, Senior Principal Scientist, CSIR-NIScPR, New Delhi.

The second session focused on building a robust ecosystem for skill development and talent generation to support the growth of India's semiconductor sector. The discussion emphasized that the success of the semiconductor ecosystem depends not only on infrastructure and investment but also on the availability of a highly skilled and industry-ready workforce capable of supporting research, design, manufacturing, and system-level integration.

Chair's Opening Remarks - Dr. Manish K. Hooda, Director (Technology), India Semiconductor Mission, MeitY, New Delhi

Dr. Manish K. Hooda from India Semiconductor Mission outlined the current status of India's semiconductor projects and the critical workforce challenges associated with them. He noted that 10 projects have been approved across multiple states, with five already commencing pilot production, including Micron Technology in Gujarat producing DRAM modules, while others are in infrastructure development stages. These projects face a common and urgent challenge: not merely the workforce needed to operate semiconductor fabs and OSAT facilities once commissioned, but also the specialized skills required during the construction phase, civil infrastructure design, cleanroom architectural standards, utility planning and integration, and the cultural discipline required to build and maintain semiconductor-grade environments

He emphasized that workforce requirements extend beyond fab operations to include construction, cleanroom design, utilities integration, and maintaining semiconductor-grade environments. The scale and specialization of skills required pose a major national challenge that cannot be met by existing training supply alone.

Dr. Hooda detailed ISM's talent strategy, which includes attracting global semiconductor professionals, engineers, scientist, promoting industry-oriented R&D, and adopting a phased training approach, domestic training followed by advanced international exposure. He also highlighted active state-level participation in semiconductor policy in addition to central government initiatives, with five states Gujarat, Assam, Odisha, Andhra Pradesh, and Punjab having approved projects.

He concluded by stressing that while the government has established policy and investment frameworks, the responsibility now lies with academia, training institutions, and industry to build a skilled workforce at scale that will make the semiconductor mission a success.

Key Highlights

- Workforce demand spans beyond fabs to construction, cleanrooms, utilities, and safety systems
- Major skill gap due to scale and specialization not met by current training capacity
- ISM strategy includes global talent attraction, industry-linked R&D, and phased training (domestic + international)
- Strong state participation alongside central initiatives (Gujarat, Assam, Odisha, Andhra Pradesh, Punjab)
- Emphasized workforce development as the foundation of the semiconductor ecosystem
- Called for academia, industry, and institutions to deliver skilled talent at scale

Expert Talk 1: NIELIT's Framework for Semiconductor Skill Development - Dr. Ripunjay Singh, Scientist E, National Institute of Electronics and Information Technology (NIELIT), New Delhi

Dr. Ripunjay Singh from National Institute of Electronics and Information Technology presented a comprehensive framework for semiconductor skill development. With an extensive national network, NIELIT is a pan-India institution with four decades of experience in training, education, and skills certification, operating 56 own centers and approximately 9,000 training partners, and having trained over 43.5 lakh people in the past five years (over 1 million in the most recent year alone). Aligned with the National Education Policy 2020, it enables seamless mobility between vocational training and formal academic programmes.

He highlighted key initiatives such as the Chip Design Associate programme, under the Wheels Design scheme targeting PCB technicians (NSQF Level 4-6); embedded systems and SoC design programmes; and fabrication-process-oriented courses covering RTL design, verification, physical design, static timing analysis, photolithography, thin film deposition, and cleanroom operations designed in consultation with

Tata Electronics, IIT faculty, and industry professionals, developed in collaboration with industry and academia. Under the Chips-to-Startup initiative, NIELIT has established smart labs and virtual VLSI platforms.

A major innovation is "Chip Craft," a cloud-based EDA platform offering complete RTL-to-GDS design flow through a browser-based interface, requiring zero software installation, supporting 500 concurrent users (scalable to one lakh), and using entirely open-source tools. This platform is specifically designed to make accessible chip design learning for engineering students at remote and non-elite institutions who cannot access proprietary EDA tools. Future plans include dedicated semiconductor skilling centres near fab sites and digital twin-based ATMP training, aiming to train one lakh professionals by 2030 across 25 semiconductor-related courses.

Main Highlights of the Presentation

- Developed a national semiconductor skilling framework, training over 43.5 lakh individuals
- Integrated education, certification, and industry-aligned training under NEP 2020
- Launched programs in chip design, embedded systems, SoC, and fabrication processes
- Introduced Chips-to-Startup initiative and Chip Craft platform for accessible chip design learning
- Chip Craft," a cloud-based EDA platform for Chip designing for engineering students
- Planned fab-linked skilling centers and aims to train 1 lakh professionals by 2030

Expert Talk 2: Prof. Awanish Pandey, Assistant Professor, Optics and Photonics Centre, IIT Delhi

Prof. Awanish Pandey from IIT Delhi highlighted the critical gaps in India's semiconductor talent ecosystem through real-world examples, showing disparities in awareness, access, and training. He emphasized the need to create inclusive and structured learning pathways for both beginners and professionals. To address this, he introduced two key initiatives: a free introductory semiconductor course on SWAYAM aimed at broad outreach, and an executive programme in Semiconductor Manufacturing and Technology for industry professionals covering physics, device design, manufacturing processes, and advanced applications. The programme is structured across four verticals: foundational physics (energy bands, carrier transport); device physics (sensors, photonic links, micro-ring resonators); manufacturing processes (CMOS process steps, tools, and cleanroom operations, constituting 50% of the course); and advanced applications (radiation-hardened electronics, photonic links for data centers).

A major concern raised was the IP gap, while Indian engineers contribute significantly to global chip design, ownership of intellectual property remains limited. He argued that this is partly a consequence of designers not deeply understanding the physical basis of the technologies they are designing for and that education which bridges device physics and manufacturing knowledge with design skills is essential for India to move from being a design service provider to an IP generating nation. Bridging design with fabrication knowledge through education is essential for India to transition from a design service provider to an IP-driven semiconductor leader.

Main Highlights of the Presentation

- Highlighted gaps in India's semiconductor talent ecosystem (awareness, access, training disparities)
- Emphasized the need for inclusive and structured learning pathways for students and professionals
- Introduced initiatives: SWAYAM introductory course and executive programme in semiconductor technology
- Covered four key areas: foundational physics, device physics, manufacturing processes, advanced applications
- Raised concern over IP ownership gap; stressed linking design with fabrication knowledge for IP-driven growth

Expert Talk 3: Strategic Roadmap for India's Semiconductor Workforce - Prof. Rishu Chaujar, Director, Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University (DTU)

Prof. Rishu Chaujar presented a structured roadmap to strengthen India's semiconductor workforce, highlighting both strengths and gaps. While India has a strong design ecosystem and a large engineering talent pool, there is a critical shortage of fabrication process engineers, ATMP specialists, and industry-ready technicians, along with limited hands-on cleanroom exposure at universities. This creates disconnect between academic training and industry requirements.

She identified key bottlenecks, including delays in land acquisition, utilities, imports, policy instability, and lack of multi-agency coordination. She recommended developing domestic capabilities in specialty materials such as photoresists, gases, and silicon wafers, along with streamlined regulatory processes. Establishing national-level cleanroom facilities and enabling shared use of existing infrastructure across institutions were emphasized.

The Centre of Excellence at Delhi Technological University was highlighted as a model integrating industry-led courses and certifications. Her roadmap includes short-term skill development and ATMP expansion, and medium-term goals of fabrication capacity, material ecosystems, and collaborative infrastructure development.

Main Highlights of the Presentation

- Highlighted strong design talent but shortage of fab engineers, ATMP specialists, and technicians
- Identified gap between academic training and industry needs, especially limited cleanroom exposure
- Pointed out bottlenecks: land delays, utilities, imports, policy instability, and approvals
- Recommended building domestic capabilities in materials (photoresists, gases, silicon wafers) and streamlined regulations
- Proposed national cleanroom facilities, shared infrastructure, and phased roadmap (short-term skilling, long-term fabrication ecosystem)

Open Discussion

The discussion highlighted the need to expand both the depth and scope of semiconductor skill development in India.

On aerospace and defense requirements, Dr. C.M. Ananda emphasized that these differ significantly from commercial semiconductor applications. They require specialized expertise in radiation-hardened design, DO-254 certification for airborne systems, and secure fabrication environments. He argued for a dedicated academic and training vertical at the postgraduate level, as these skills cannot be developed through standard semiconductor programs. Dr. Hooda agreed, noting that SCL Mohali already leads in radiation-hardened technologies and that current ISM-linked curricula include elements such as radiation-hardened design and Process Design Kit (PDK) development. He also stressed that DO-254 compliance must be integrated from the design stage itself.

Broadening the perspective, Dr. Sujit Bhattacharya pointed out that semiconductor success depends not only on engineers but also on ecosystem enablers such as technology lawyers, financial experts, and business professionals. He highlighted that many Indian deep-tech startups struggle with commercialization due to gaps in these areas. Supporting this view, Dr. Hooda noted that institutions like IIT Delhi are introducing interdisciplinary programs covering IP, valuation, and semiconductor economics, recognizing that such ecosystem skills are essential alongside technical expertise.

Closing Remarks: Dr. Manish K. Hooda

Dr. Hooda's closing remarks affirmed that skilled workforce development is the foundational requirement for a sustainable semiconductor manufacturing ecosystem encompassing not only fab and OSAT operations but also utility infrastructure, safety systems, and civil construction. He called on all institutional stakeholders, universities, training bodies, R&D laboratories, and industry to accept their share of responsibility for delivering the workforce the mission requires. He noted that the government has discharged its policy and investment responsibility; the obligation now rests with institutions to operationalize the training architecture and produce work-ready talent at scale. The session closed with felicitation of speakers and the announcement of a lunch break.

Key Insights

Workforce as the Foundation of the Semiconductor Ecosystem

- Semiconductor growth depends critically on a highly skilled, industry-ready workforce.
- Skill requirements span design, fabrication, packaging (OSAT), infrastructure, and system integration.
- Workforce demand includes not only operational roles but also construction, cleanroom design, and utility management.

Urgent Skill Gap across the Value Chain

- India faces a shortage of fabrication engineers, ATMP specialists, and cleanroom technicians.
- Existing training systems are insufficient to meet the scale and specialization required.
- Many graduates lack hands-on exposure to semiconductor manufacturing processes.

Scaling Training through Digital and Hybrid Models

- Virtual labs and cloud-based platforms (e.g., chip design simulation tools) can democratize access.
- Training programmes aim to reach Tier 2 and Tier 3 institutions with limited infrastructure.
- Hybrid models combining online learning practical exposure are essential.

Need for Industry-Aligned Curriculum

- Courses must integrate design, device physics, and manufacturing knowledge.
- Strong emphasis on industry-designed curricula, micro-credentials, and certification programmes.
- Bridging theory with practice is key to producing job-ready engineers.

Importance of Hands-On and Cleanroom Training

- Lack of cleanroom infrastructure is a major bottleneck in skill development.
- Shared facilities and collaborative use of existing labs (e.g., IITs) are recommended.
- Practical fabrication experience is essential even at a basic level (e.g., diode fabrication).

Multi-Level Talent Development Strategy

- Training must span entry-level technicians to advanced researchers and global experts.
- Strategy includes domestic training + international exposure for advanced skills.
- Long-term goal: build a globally competitive semiconductor talent pool.

Expanding the Definition of Semiconductor Skills

- Ecosystem requires non-technical roles: IP lawyers, technology financiers, policy experts.
- Business, legal, and financial expertise is critical for commercializing deep-tech innovations.

Strengthening Academia–Industry Linkages

- Collaboration is essential for curriculum design, internships, and applied research.
- Industry participation ensures relevance and employability of graduates.

Infrastructure and Policy Bottlenecks

- Challenges include regulatory approvals, power/water supply, and import delays.
- Need for single-window clearance systems and stable long-term policies.

Strategic Roadmap for Talent Development

- Short-term: Expand training programmes, strengthen design ecosystem, scale ATMP skills.
- Medium-term: Develop fabs, materials ecosystem, and semiconductor clusters.
- Long-term: Position India as a global semiconductor talent and manufacturing hub.

Specialized Skill Tracks for Strategic Sectors

- Aerospace and defense require distinct skill sets (e.g., radiation-hardened design, certification standards like DO-254).
- Dedicated advanced-level training programmes are necessary for such sectors.

Shared Responsibility across Stakeholders

- The government has provided policy and investment frameworks.
- Responsibility now lies with universities, training institutions, industry, and R&D labs to deliver talent at scale.

List of Experts in the session

1. Dr. Manish K. Hooda, Director (Technology), India Semiconductor Mission (ISM), MeitY, New Delhi –Chairman
2. Dr. Bornali Sarma, Senior Principal Scientist, CSIR-NIScPR, New Delhi-Co-Chairman
3. Dr. Ripunjay Singh, Scientist E, NIELIT (National Institute of Electronics and Information Technology, New Delhi)
4. Prof. Awanish Pandey, Assistant Professor, Optics and Photonics Centre, IIT Delhi
5. Prof. Rishu Chaujar, Director of the Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University (DTU), New Delhi

Session III: Policy, Governance & Institutional Framework

Highlights of the session

This session was chaired by Prof. Sujit Bhattacharya, Adjunct Professor, Amrita University & Former Chief Scientist, CSIR-NIScPR and Co-Chaired by Dr. Vipan Kumar, Chief Scientist & Head (Energy Environment & Sustainability Division), CSIR-NIScPR, New Delhi.

The third session focused on the policy environment, governance mechanisms, and institutional frameworks necessary to support the development of a strong semiconductor ecosystem in India. The discussion highlighted that sustained growth in this strategic sector requires coordinated policy support, effective institutional mechanisms, and long-term governance structures that enable collaboration among government, industry, and research institutions. The session emphasized that effective policy design, transparent governance, and strong institutional coordination are essential to building a sustainable semiconductor ecosystem.

Expert Talk 1: Semiconductor Requirements for Aerospace and Defense: Policy and Regulatory Imperatives - Dr. C.M. Ananda, Programme Director for Civil Aircraft Programme, Chief Scientist & Head, Aerospace Electronics Division, CSIR-NAL, Bengaluru

Dr. C.M. Ananda brought a distinctive sectoral perspective to the workshop by focusing on the specific semiconductor requirements, risk profiles, and policy gaps pertaining especially for strategic sectors like aerospace and defense. He emphasized the critical role of semiconductors in avionics systems across programmes such as HANSA, SARAS, RTA Programme, and High Altitude Pseudo-Satellite (HAPS). Unlike commercial applications, aerospace systems demand extremely high reliability, safety, and long-term stability, with semiconductor components often remaining fixed for over 30 years once certified.

He identified key risks, including supply chain disruptions due to geopolitical factors, counterfeit chips with embedded malware or unknown code from untrusted fabs (which certification authorities cannot accept on any aerospace platform); FPGA specific risks including bitstream tapping, tool dependency, and foundry concentration; absence of IP and design rights for long duration programmes; and the comprehensive tool chain dependency, even an 'indigenous' design is embedded within a host of imported tools, compilers, and bitstream generators whose internals are unknown to the user, limited transparency, and heavy reliance on imported software and hardware ecosystems.

To address these challenges, Dr. Ananda proposed a comprehensive policy framework focused on achieving semiconductor self-reliance in strategic sector like aerospace. This includes establishing a 'National Semiconductor Authority' with defined programmes for industry participation and active R&D, developing a dedicated certification and regulatory framework for aerospace-grade semiconductors certification, and a trusted foundry in India meeting security, safety, and screening standards.

A centralized national verification and security mechanism may be established to validate chip integrity, detect vulnerabilities, and ensure compliance with aerospace and defense safety requirements. Such regulatory systems will be essential to ensure that domestically developed semiconductors can be safely deployed in mission-critical platforms. In addition, there is a need to establish trusted domestic semiconductor foundries that meet strict security and reliability standards. There is also needs to create 'specialized certification standards' for aerospace-grade and defense-grade semiconductors.

Dr. Ananda also called for a consistent, long-term semiconductor policy, emphasizing that policy stability over 10-15 years is essential for aerospace programmes given their multi-decade lifecycles. He stressed the importance of building full-stack indigenous capabilities across chip design, fabrication, tools, and testing.

He also emphasized the need for long-term policy stability aligned with multi-decade aerospace programme lifecycles and called for coordinated efforts within CSIR through domain-specific clusters to integrate research outputs into the national semiconductor mission.

Main Highlights of the Presentation

- Highlighted unique and stringent semiconductor requirements for aerospace and defense systems
- Emphasized need for high reliability, safety, and long lifecycle stability (30+ years)
- Noted critical role of semiconductors in avionics systems (HANSA, SARAS, RTA, HAPS)
- Semiconductor policies should remain stable for at least 10–15 years to support sustained investment, infrastructure development, and long-term research, especially considering the long lifecycle of aerospace and defense systems
- Proposed to establishment of a 'National Semiconductor Authority' to coordinate semiconductor policy, R&D programmes, industry participation, and long-term strategic planning, particularly for critical sectors such as aerospace, defense, and advanced digital technologies

- A robust regulatory and verification framework must be developed to ensure reliability, security, and performance of the chips for strategic sector like aerospace and defense
- A centralized national verification and security mechanism may be established to validate chip integrity, detect vulnerabilities, and ensure compliance with aerospace and defense safety requirement
- Emphasized need for trusted domestic foundries, full-stack capabilities, and coordinated CSIR efforts
- Stressed the importance of building full-stack indigenous capabilities across chip design, fabrication, tools, and testing
- Raised concerns over counterfeit chips, FPGA vulnerabilities, and lack of transparency
- Pointed out absence of domestic IP ownership and design control

Expert Talk 2: Innovation Systems, Policy Coherence and the Semiconductor Ecosystem - Prof. Sujit Bhattacharya, Adjunct Professor, Amrita University & Former Chief Scientist, CSIR-NIScPR

Prof. Sujit Bhattacharya presented a systems-based perspective on semiconductor development, emphasizing that India's semiconductor mission must be understood within the broader science, technology, and innovation (STI) ecosystem. He argued that the key challenge is not just technological capability but the effective translation of scientific knowledge into economic value through well-coordinated institutions, policies, norms, and governance mechanisms that together enable or inhibit the movement of knowledge from laboratory to market. The India Semiconductor Mission, he noted, should be continuously evaluated through adaptive policy frameworks rather than treated as a standalone initiative.

Drawing on global examples from the US, Japan, South Korea, and Taiwan, he showed that successful semiconductor ecosystems are built on strong knowledge institutions, corporate research laboratories, and robust university–industry linkages that provided the knowledge infrastructure for technology translation that provided the knowledge infrastructure for technology translation. He particularly emphasized Japan's model, particularly its banking sector, which provided non-dilutive, patient, long-term funding. The shift from purely linear innovation models (basic research → applied research → commercialization) to more complex, quadruple-helix models incorporating civil society, user communities, and multiple feedback loops were identified as a defining feature of successful contemporary innovation systems.

He concluded by stressing the need for evidence-based policy learning, institutional mechanisms for collaboration, university-industry linkages, and continuous innovation in policy design to ensure long-term success.

Main Highlights of the Presentation:

- Emphasized knowledge-to-market translation as the core challenge, not just technology capability
- Highlighted disconnect between R&D, STI, and production ecosystems
- Stressed importance of institutions, governance, incentives, and feedback mechanisms

- Recommended adaptive and continuously evaluated policy frameworks for ISM
- Drew lessons from US, Japan, South Korea, and Taiwan models
- Highlighted role of strong knowledge institutions and university–industry linkages
- Emphasized Japan's patient, non-dilutive funding model
- Advocated shift to quadruple-helix innovation model (beyond linear approach)
- Called for evidence-based policymaking and continuous policy innovation

Expert Talk 3: Comparative Analysis of Global Semiconductor Policies - Dr. Shiv Narayan Nishad, Principal Scientist, CSIR-NIScPR, New Delhi

Dr. Shiv Narayan Nishad presented a comparative analysis of global semiconductor policies across major economies including the United States, China, Taiwan, South Korea, Japan, Germany, Singapore, and Israel, with the aim of identifying best practices and policy gaps for India. He traced India's semiconductor journey of India from early institutional foundations such as Bharat Electronics Limited, CSIR-CEERI, and SCL Mohali, to the recent initiatives like India Semiconductor Mission (ISM 1.0) with a ₹76,000 crore incentive framework, Semicon India programme. .

Drawing lessons from global leaders, he highlighted the importance of strong institutional coordination, and coordinated industrial strategies as key success factors. The United States was highlighted for establishing the National Semiconductor Technology Centre (NSTC) in 2022 as a federal coordination hub spanning government, industry, and academia; the CHIPS Manufacturing USA institutes (16 regional institutes for advanced packaging, metrology, manufacturing, and workforce); the Semiconductor Research Corporation (SRC, 1982) as an industry-funded pre-competitive research consortium linking universities to chip companies; and the CHIPS and Science Act (2022) funding for R&D, workforce development, and advanced packaging. Taiwan's long-term cluster strategy (Hsinchu Science Park) and strong academia-industry project linkages were noted as foundational. Japan's role of non-dilutive bank financing and consumer-market orientation was flagged. South Korea and Germany's coordinated national industrial policy mechanisms were also referenced.

Dr. Nishad emphasized that India must strengthen its institutional architecture, scale advanced packaging (ATMP/OSAT), expand design incentives, and accelerate semiconductor cluster development. He also proposed establishing an 'India Semiconductor Research Centre' and advancing "semiconductor diplomacy" to enable global collaboration, technology transfer, and supply chain integration for long-term ecosystem growth.

Main Highlights of the Presentation

- Presented comparative analysis of global semiconductor policies across major economies

- Highlighted importance of strong institutional coordination and industrial strategy
- Emphasized need to strengthen India's institutional architecture
- Recommended scaling ATMP/OSAT, design incentives, and semiconductor clusters
- Proposed India Semiconductor Research Centre and semiconductor diplomacy for global integration

Expert Talk 4: India's Semiconductor Ecosystem: Innovation, AI, and Strategic Opportunity - Ms. Naba Suroor, Science, Technology and Innovation Mission Division, NITI Aayog, New Delhi

Ms. Naba Suroor presented a policy-oriented overview of India's semiconductor ecosystem, highlighting market potential, structural challenges, and emerging opportunities in AI-driven semiconductors. She noted that the global semiconductor market is expected to exceed USD 1 trillion by 2030, with India's market projected at USD 150 billion, including a USD 21 billion share in the rapidly growing AI semiconductor segment by 2030

She emphasized that geopolitical shifts and rising costs in China are creating opportunities for India to integrate into global supply chains. She also highlighted that US firms account for approximately 71.5% of global semiconductor market value, driven by dominance in chip design, IP, and software tools, a configuration that reinforces the importance of India building IP-centric design capability.

Government support through the India Semiconductor Mission includes fiscal incentives across the value chain, support for fabs, ATMP/OSAT facilities, and design-linked incentives, together covering the full semiconductor value chain. Despite over 100 semiconductor startups, she pointed out a critical gap in intellectual property, with only a small proportion of startups are working on proprietary intellectual property.

Ms. Suroor identified four principal challenges: the technology gap (India's fabrication capabilities are largely at 40 nanometers and above while global leaders operate below 5 nanometers, requiring USD 4-5 billion per fab to bridge), global market entry barriers (competition from established players requiring improvements in technology readiness, cost efficiency, and workforce), material dependencies (advanced semiconductor manufacturing relies on high-purity imported materials exposing India to supply disruption), and low R&D intensity and weak IP protection frameworks. She argued that semiconductor capability is not merely an industrial priority but a strategic imperative for national security, digital infrastructure, and financial returns across the economy.

She highlighted AI semiconductors as a major opportunity area, including edge AI chips, AI-specific SoCs, ; customized chips optimized for targeted AI workloads, AI-enabled advanced semiconductor packaging, cloud-based AI infrastructure; and FPGA-based solutions for real-time processing. She concluded that strengthening IP, R&D, and ecosystem integration is essential for India to emerge as a competitive global semiconductor and AI innovation hub.

Main Highlights of the Presentation

- Presented policy overview of India's semiconductor ecosystem and future potential
- Highlighted market projections: $1 trillion global, $150 billion India, $21 billion AI segment by 2030
- Identified geopolitical shifts (China+1) as opportunity for global supply chain integration
- Outlined government support under ISM (fabs, ATMP/OSAT, design-linked incentives)
- Noted IP gap despite 100+ startups; limited focus on core innovation
- Identified challenges: technology gap, high capital costs, import dependence, market entry barriers
- India has semiconductor clusters across multiple states and over 100 startups, but only about one-third focus on proprietary IP
- Need to strengthen IP, R&D, and ecosystem integration for global competitiveness
- Low R&D investment and weak IP frameworks limit long-term competitiveness of the ecosystem
- Key barriers include global competition, cost and technology readiness challenges, and dependence on imported high-purity materials
- Emphasized AI semiconductors as a key opportunity area
- High-value opportunities for startups lie in edge AI chips, AI-specific SoCs, customized AI hardware, advanced packaging, cloud AI infrastructure, and FPGA-based solutions

Expert Talk 5: Geopolitics, Raw Materials, and India's Strategic Semiconductor Imperative - Dr. Amit Kumar, Assistant Professor, Research and Information System for Developing Countries (RIS), New Delhi

Dr. Amit Kumar presented a geopolitical and resource-centric perspective on India's semiconductor strategy, emphasizing the urgency of achieving self-reliance. He traced India's early progress through the establishment of the Semiconductor Laboratory (SCL), noting that the country was once close to global technological parity before a major disruption in 1989 halted momentum, resulting in a decades-long gap.

He highlighted India's current dependence on imports, with around 90% of chips sourced externally, 70% from China, and annual imports reaching approximately ₹1.5 lakh crore. With rapidly growing demand driven by smartphones, AI, and digital infrastructure, semiconductor capability has become a strategic necessity. India's ambitions in the Digital India, India AI, and Quantum missions makes strategic self-reliance not merely desirable but economically and politically imperative. He noted that India's strength in chip design and the focus of the Design-Linked Incentive (DLI) scheme are important entry points for building domestic capacity as India's demonstrated global talent in chip design.

A key contribution of his talk was the focus on raw material geopolitics. Critical semiconductor materials and rare earth elements are concentrated in a few countries, with China dominating global processing capacity. This creates significant supply risks that cannot be addressed by manufacturing alone.

Dr. Kumar argued that the Ministry of External Affairs has a direct and essential role to play in semiconductor strategy: through bilateral and multilateral diplomatic engagements to secure access to critical material supply chains, negotiate technology transfer arrangements, and build the foreign policy architecture supporting India's semiconductor ambitions.

Main Highlights of the Presentation

- Presented a geopolitical and resource-centric perspective on semiconductor strategy
- Traced India's early progress via SCL and setback after the 1989 disruption
- Today, ~90% of India's chips are imported, with ~70% coming from China, totaling about ₹1.5 lakh crore annually
- Rapid domestic demand driven by smartphones, AI data centres, and national tech missions makes self-reliance economically and strategically critical
- Emphasized semiconductors as a strategic and economic necessity
- India's strength in chip design aligns with the Design-Linked Incentive scheme, targeting the segment that captures ~50% of semiconductor value
- A major overlooked challenge is raw material geopolitics, with critical minerals concentrated in a few countries
- Noted concentration of rare earths and processing capacity in few countries (esp. China)
- Semiconductor strategy must extend beyond manufacturing to diplomacy, with the Ministry of External Affairs playing a key role in securing materials, partnerships, and technology access

Open Discussion

The discussion emphasized the importance of sector-specific strategies, value-chain positioning, and institutional alignment in India's semiconductor ecosystem.

On aerospace and defense policy, Dr. Bhattacharya supported the view that this sector has unique requirements such as stringent certification, long-term supply reliability, trusted fabrication, and security safeguards. He agreed that these needs demand a separate regulatory and policy framework, distinct from the commercial ISM approach.

In the manufacturing vs. design debate, it was noted that while design and IP capture the highest value, manufacturing remains critical for strategic sectors. The U.S. model demonstrates that sensitive components like aerospace chips and sensors are always domestically produced. India, therefore, should not rely solely on outsourced manufacturing models but instead develop niche strengths at key points in the value chain, while ensuring domestic production for security-critical technologies.

On policy coherence, participants highlighted the need for CSIR to reposition itself as a bridge institution, focusing on scaling technologies from mid to higher TRL levels. This would require an internal policy shift, aligning with its long-term vision to support innovation translation rather than competing with academia.

Closing Remarks

Dr. Bhattacharya closed the session by observing that the five presentations had collectively demonstrated the multi-dimensional nature of the semiconductor policy challenge: it encompasses not only technology and manufacturing investment, but also innovation governance, sectoral regulation, comparative policy learning, AI-specific strategy, and geopolitical raw material diplomacy. He highlighted that the workshop had surfaced a set of recommendations that were both granular and cross-cutting.

Key Insights of the Session

Strategic Policy & Governance

- Strong policy support and adaptive governance frameworks identified as critical
- Need for dedicated regulatory structures, especially for strategic sectors like aerospace and defense
- Recommendation for establishment of institutions such as the National Semiconductor Authority to coordinate semiconductor policy, R&D programmes, industry participation, and long-term strategic planning, particularly for critical sectors such as aerospace, defense, and advanced digital technologies
- Importance of long-term policy stability (10–15 years) aligned with industry lifecycles to support sustained investment, infrastructure development, and long-term research, especially considering the long lifecycle of aerospace and defense systems
- Stressed the importance of institutional coordination and positioning organizations like Council of Scientific and Industrial Research as key enablers of technology translation.

Regulatory Framework and Strategic Sector Security

- Given the critical importance of semiconductors in a strategic sector like aerospace and defense systems, a robust regulatory and verification framework must be developed to ensure reliability, security, and performance.
- A specialized certification and regulatory framework may be introduced for semiconductors used in strategic sectors. This framework must define strict standards for safety, reliability, and security.
- A centralized national verification and security mechanism may be established to validate chip integrity, detect vulnerabilities, and ensure compliance with aerospace and defense safety requirements.
- Need to establish trusted domestic semiconductor foundries that meet strict security and reliability standards
- Needs to create 'specialized certification standards' for aerospace-grade and defense-grade semiconductors

Innovation & Ecosystem Development

- Identified knowledge-to-market translation as a key bottleneck in India's semiconductor journey.
- Requires strong institutions, governance, incentives, and university–industry linkages, with adaptive and evidence-based policymaking.
- Advocated for advanced innovation models (quadruple-helix) and continuous policy learning.
- Highlighted need to boost R&D intensity, intellectual property (IP) creation, and indigenous capabilities.

Global Insights & Strategic Positioning

- Drew lessons from global leaders such as United States, Japan, South Korea, and Taiwan on institutional strength, funding models, and industry coordination.
- Successful countries rely on coordinated industrial strategies, patient financing, and strong knowledge ecosystems
- India must strengthen institutional architecture, semiconductor clusters, design incentives, and advanced packaging capabilities
- Recommended strengthening semiconductor clusters, scaling ATMP/OSAT, and establishing an India Semiconductor Research Centre.
- Highlighted importance of semiconductor diplomacy for global integration and technology access.

Technology, Manufacturing, Market Opportunity and Ecosystem Gaps

- Noted strong market potential: global semiconductor market projected at $1 trillion and India at $150 billion by 2030.
- Key gaps include low R&D investment, weak IP development, and limited focus on core innovation despite 100+ startups

- Identified gaps in fabrication technology, design ownership, and dependence on foreign ecosystems.
- Highlighted government support through the India Semiconductor Mission across the value chain.
- Emphasized scaling manufacturing, design incentives, and full value-chain participation.

AI & Emerging Growth Areas

- Identified AI semiconductors as a key opportunity segment for India.
- Highlighted domains such as edge AI chips, AI SoCs, custom chips, and advanced packaging.
- Stressed importance of building IP-driven design capabilities to capture higher value.
- Leveraging geopolitical shifts (China+1) for integration into global supply chains.

Geopolitics, Supply Chains & Strategic Risks

- Highlighted high import dependence and supply chain vulnerabilities, particularly linked to China.
- Emphasized importance of securing critical raw materials and rare earth supply chains.
- Reinforced semiconductor self-reliance as a strategic and economic necessity.
- India imports ~90% of chips, with heavy dependence on China and critical raw material concentration globally
- Semiconductor strategy must include diplomacy, supply chain partnerships, and technology access, making it a national strategic priority

Sector-Specific Priorities (Aerospace & Defense)

- Identified unique requirements: high reliability, long lifecycle (30+ years), and strict certification standards.
- Highlighted risks from counterfeit chips, foreign toolchains, and lack of trusted fabs.
- Recommended dedicated regulatory frameworks, certification systems, and domestic trusted foundries.
- Emphasized need for full-stack indigenous semiconductor capabilities for strategic sectors.

International Cooperation and Semiconductor Diplomacy

- Emphasized on strengthening international cooperation and semiconductor diplomacy
- Attract global investments, supporting cross-border industrial collaborations, and positioning India as a reliable partner in semiconductor manufacturing and technology development
- Integrating foreign policy objectives with the national semiconductor development strategy that may further strengthen India's ability to build strategic alliances, access critical technologies, and enhance its role in the evolving global semiconductor landscape

List of Experts in the session

1. Prof. Sujit Bhattacharya, Adjunct Professor, Amrita University & Former Chief Scientist, CSIR-NIScPR -Chairman
2. Dr. Vipan Kumar, Chief Scientist & Head (Energy Environment & Sustainability Division), CSIR-NIScPR, New Delhi-Co-Chairman

1. Dr. C.M. Ananda, Chief Scientist & Head, CSIR-NAL, Bengaluru;
2. Prof. Sujit Bhattacharya, Adjunct Professor, Amrita University & Former Chief Scientist, CSIR-NIScPR, New Delhi
3. Dr. Shiv Narayan Nishad, Principal Scientist, CSIR-NIScPR, New Delhi
4. Ms. Naba Suroor, Science, Technology and Innovation Mission Division, NITI Aayog, New Delhi
5. Dr. Amit Kumar, Assistant Professor, Research and Information System for Developing Countries (RIS), New Delhi

Panel Discussion on "Strategic Pathways: A roadmap for India's Semiconductor Future

Highlights of the Session

Session chaired by Prof. Navakanta Bhat, Dean, Division of Interdisciplinary Science; Professor, Centre for Nanoscience and Engineering, IISc Bengaluru (joined through Video Conference mode) and Co-Chaired **by** Dr. Sujit Bhattacharya, Adjunct Professor at Amrita University & Former Chief Scientist, NIScPR, New Delhi.

The panel discussion on "Strategic Pathways: A Roadmap for India's Semiconductor Future" brought together experts from industry, research institutions, and semiconductor companies to deliberate on the key actions required to strengthen India's semiconductor ecosystem. The discussion focused on identifying practical strategies for advancing the country's capabilities across design, manufacturing, research, and talent development in order to achieve long-term technological self-reliance.

Chair's Opening Remarks - Prof. Navakanta Bhat, Dean, Division of Interdisciplinary Science and Professor, Centre for Nanoscience and Engineering, Indian Institute of Science (IISc) Bengaluru

Prof. Navakanta Bhat opened the panel discussion by contextualizing the workshop within his three decades in the semiconductor domain. He affirmed that the current moment, the alignment of ISM, private industry investment, central and state government initiatives, and global supply chain realignment is unprecedented. He noted that semiconductors and electronics were identified as one of eleven thematic areas at the inaugural ESTIC-2025 (Emerging Science, Technology and Innovation Conclave), reflecting the highest level of government recognition. The ecosystem, he observed, spans from materials at one extreme through processes, equipment, chips, packages, systems, and solutions, a uniquely complex, interdisciplinary, and fast-moving domain. He framed the panel's task as moving from diagnosis to prescription: what must be done, by whom, and in what sequence, to realize 'Viksit Bharat 2047' through semiconductor self-reliance.

Panelist: Dr. Roopa Hegde, Lead Engineer, Semiverse Solutions, Lam Research

Dr. Roopa Hegde, representing Lam Research India (25 years of operations in India), presented the Semiconductor Skills Development Programme, a tripartite initiative with ISM and IISc Bengaluru targeting training of over 60,000 engineers over the next decade. The programme's central innovation is the deployment of SEMulator3D, Lam Research's flagship virtual semiconductor fabrication tool, to deliver process-integration training at scale. Key outcomes: up to 90% cost saving per trainee compared to physical cleanroom training; elimination of exposure to hazardous chemicals and gases; and reach extended to Tier 2 and Tier 3 cities across India.

Launched as a pilot with IISc students in 2024, the programme has expanded to 81 university partnerships. ISM funds operational costs; IISc delivers a train-the-trainer model, equipping professors from partner universities to upskill their own students. Lam Research provides ongoing technical support through regular meetings with all 81 trained faculty. Dr. Hegde's closing formulation captured the programme's philosophy: for the large population of engineers who will never access a physical fab during their education, virtual simulation training represents 'something is better than nothing', a critical baseline of fabrication literacy that physical infrastructure alone cannot provide at a national scale.

Panelist: Dr. Hemang Shah, Senior Director, Government Affairs and Business Development, Applied Materials India, Bengaluru, Karnataka

Dr. Hemang Shah, joined online from Applied Materials India framed India's strategic opportunity as capturing 'the missing middle', the gap between India's established strengths in chip design and consumption and its currently limited role in manufacturing, materials, and equipment. He identified three technology driven demand trends: the exponential growth of AI, which is driving fundamental device architectural changes in response to rising power consumption; the rise of data centres, which are major semiconductor consumers demanding both high performance and energy efficiency; and the emergence of chiplet architectures offering modular innovation pathways. He emphasized that semiconductor equipment manufacturing is inherently interdisciplinary, drawing on mechanical engineering, chemistry, physics, electrical, and electronics expertise, a talent profile India's engineering institutions are well-positioned to supply. He emphasized for ecosystem-wide R&D investment and collaboration encompassing industry and academia jointly, and stressed the critical importance of building a domestic supplier base: companies supplying specialty chemicals, precision machining, and components that highlight the semiconductor ecosystem at every level. The Ministry of Electronics and Information Technology of India (MeitY) has outlined the importance of incentivizing such collaboration, he noted, and this is the right moment to act.

Panelist: Dr. Manish Matthew, Senior Principan Science, Head TDB, & Head Semiconductor Diamond Research Group (DRG), CSIR-CEERI Pilani

Dr. Manish Matthew described CSIR-CEERI Pilani's four decade semiconductor journey: silicon devices in the early 1980s, MEMS in the 1990s, compound semiconductors from 2010, and most recently diamond-on-silicon and diamond-on-GaN integration for EV and next-generation power device applications. He raised a specific and important structural gap in ISM 1.0: the mission did not include a provision for R&D organizations. When industries approached CSIR-CEERI to collaborate on LED technology for ISM, the application was refused because ISM 1.0 required technology to originate from an external source, domestically developed R&D technology was ineligible. Dr. Matthew expressed confidence that ISM 2.0 will include an explicit R&D vertical, enabling industry-laboratory collaborations to access mission support. On training, he highlighted CSIR-CEERI's two-week residential semiconductor fabrication programme, in which participants undertake actual wafer processing and produce a complete diode providing the practical manufacturing experience absent from most academic curricula. He provided the information about the Surat Microwave Plasma Chemical Vapor Deposition (MPCVD) reactor cluster as evidence of India's intrinsic manufacturing ingenuity: Surat's lab-grown diamond industry, having procured one reactor from Japan, independently replicated it, with companies now routinely operating 150-200 domestically made MPCVD reactors each. Dr. Bhattacharya contextualized this as an example of learning by doing innovation in industrial clusters, legitimate as a learning mechanism, distinct from IP infringement, and worthy of study as a model for semiconductor equipment development.

Panelist: Mr. George Paul, Director, Government Relations & Corporate Strategy, Sahasra Semiconductors Pvt. Ltd, New Delhi

Mr. George Paul, representing Sahasra Semiconductors Pvt Ltd - India's first operational memory and semiconductor IC packaging company (operational ten months, shipping DRAM, RFID, and eSIM chips to over ten countries from Bhiwadi near Delhi), provided a strategic and historical perspective drawing on 44 years in the electronic hardware industry. He started his talk with quotation of the statement of Dr. V.K. Saraswat of NITI Aayog- 'Nothing is beyond India's ability', whenever India has set a goal, assured the demand, and put in the funding, we have successfully overcome all hurdles and built the technology and products we need. He offered the Hero Honda & Hero MotoCorp evolution as the relevant industrial analogy: starting from a technology collaboration in 1981-82, the company progressively internalized engineering capability and now dominates motorcycle markets in Africa, markets that Chinese competitors have been unable to penetrate. His signature strategic contribution was the vision of India transitioning from a service economy to a knowledge economy or more precisely, an IP economy. He illustrated the economics with two vivid examples: a consumer paying ₹10 for a bottle of Coke automatically remits ₹1 as brand royalty to the US; a buyer paying ₹90,000 for a laptop automatically remits ₹10 as HDMI consortium royalties. This is the compounding, scalable economic power of IP ownership. Sahasra's internal philosophy 'Mind India', the power of the Indian mind to create intellectual property that generates perpetual economic returns. He emphasized that NITI Aayog may develop a formal policy framework for a knowledge/IP economy, arguing that India's greatest national asset - intellectual capital is systematically under-monetized.

Panelist: Shri Rajendra Pratap, Vice President, VerseSemi Microelectronics Pvt. Ltd, Noida

Shri Rajendra Pratap, Vice President at VerseSemi Microelectronics (a fabless analog and mixed-signal IC design company in Noida, India), proposed two targeted policy recommendations. First, he proposed for policy level incentives to promote adoption of indigenous semiconductor components, creating a competitive playing field for domestic manufacturers against established Chinese imports. Knowledge awareness campaigns and adoption incentives would generate initial market traction and reduce the credibility disadvantage that early-stage domestic manufacturers face. Second, he addressed the question of capability sequencing and the legitimate use of open standards as a learning pathway. He drew a careful legal and strategic distinction: implementing a technology independently from publicly available specifications, as is routinely done for open standards such as USB and HDMI is legally permissible and strategically important for building domestic capability. He framed this as a necessary developmental phase: India's semiconductor companies must rise to a competitive capability level before global players will engage as peers using the analogy of a new badminton player who must develop sufficient skill before established players will agree to compete.

Open Discussion

The discussion highlighted the delicate balance between intellectual property (IP) protection and learning-by-doing in industrial growth. Dr. Bhattacharya clarified that while learning from existing technologies is legitimate, infringement is not. He warned that increasingly restrictive global IP regimes, such as patent pools and opaque licensing, limit developing countries' ability to build capabilities. Mr. George Paul stressed that unlike earlier decades, reverse engineering is no longer viable; India must focus on open innovation and generating original IP. The Surat MPCVD example was reframed as learning-by-doing through first-principles understanding, not imitation.

On India's development path, panelists emphasized achieving full-stack capability, from design to manufacturing and delivery. Despite strong design talent, India captures limited value without IP ownership and product branding. Coordinated efforts across semiconductor manufacturing, design incentives, and knowledge-economy policies are essential for long-term competitiveness and value creation.

Key Insights

- India is at a critical inflection point, with strong alignment between government initiatives, private investment, and global supply chain shifts creating a unique opportunity for semiconductor growth.
- The semiconductor ecosystem is highly complex and interdisciplinary, spanning materials, fabrication, packaging, and systems, requiring coordinated development across all segments.

Strategic Context and Opportunity

- Current moment is unprecedented, with alignment of government policy (ISM), industry investment, and global supply chain shifts creating a unique opportunity for India
- Semiconductors span a complex, end-to-end ecosystem (materials to systems), requiring coordinated, interdisciplinary action to achieve Viksit Bharat 2047

Skills Development and workforce readiness

- Large-scale training initiative aims to skill 60,000+ engineers using virtual fabrication tools like SEMulator3D
- Virtual training enables 90% cost reduction, wider access (including Tier 2/3 cities), and safer learning without cleanroom exposure
- Train-the-trainer model with universities ensures scalable and sustained talent development

Ecosystem & Industrial Strategy

- India must address the "missing middle", gaps in manufacturing, materials, and equipment.
- India's opportunity lies in bridging the gap between design strength and weak manufacturing/material capabilities
- Growth drivers include AI, data centres, and chiplet architectures, requiring new device innovations
- Strong need to build a domestic supplier ecosystem (materials, components, precision manufacturing)

Role of R&D and Innovation

- Earlier policy frameworks had limited integration of R&D institutions, restricting collaboration and innovation. ISM 1.0 lacked direct support for R&D institutions, limiting industry–lab collaboration
- Future policy (ISM 2.0) must integrate R&D organizations into the semiconductor mission
- Practical training and learning-by-doing models (e.g., fabrication programs, Surat cluster innovation) are critical for capability building
- India has demonstrated potential through learning-by-doing and cluster-based innovation models.
- Hands-on fabrication training is necessary to bridge the gap between theory and practice.

IP and Knowledge Economy

- India must transition from a service-led economy to an IP-driven knowledge economy.
- Ownership of patents, standards, and product brands is essential for long-term value capture.
- National policy focus needed to monetize India's intellectual capital effectively.

Policy & Market Development

- Need for policy incentives to promote adoption of indigenous semiconductor products
- Domestic semiconductor products face credibility and adoption barriers in early stages.

- Policy incentives and awareness programmes can help drive initial adoption.
- Open standards and learning-by-doing should be encouraged as legitimate capability-building pathways.

IP, Open Innovation, and Learning-by-Doing

- Clear distinction between legitimate learning and IP infringement in industrial development
- Traditional reverse engineering is less viable; focus must shift to open innovation and original IP creation
- Increasingly restrictive **global IP regimes pose barriers for developing countries**

Path to Full-Stack Semiconductor Capability

- India must move beyond design to end-to-end capability (design → fabrication → packaging → testing → products)
- Strong consensus on achieving full-stack semiconductor capability (design to product).
- Current strength in design talent (~20% globally) does not translate into proportional economic value without IP ownership
- Coordinated approach needed across manufacturing, design incentives, and knowledge economy frameworks
- Need for policy coordination across manufacturing, design incentives, and IP frameworks.
- Long-term success depends on integration of talent, innovation, manufacturing, and global collaboration.

List of Panelists:

1. Prof. Navakanta Bhat, Dean, Division of Interdisciplinary Science; Professor, Centre for Nanoscience and Engineering, IISc Bengaluru (joined through Video Conference mode)-Chairman
2. Dr. Sujit Bhattacharya, Adjunct Professor at Amrita University & Former Chief Scientist, NIScPR, New Delhi-Co-Chairman
3. Dr. Roopa Hegde, Lead Engineer, Lam Research India;
4. Dr. Hemang Shah, Senior Director, Government Affairs and Business Development, Applied Materials India (online)
5. Dr. Manish Matthew, Senior Principal Scientist, CSIR-CEERI Pilani
6. Mr. George Paul, Director, Government Relations and Corporate Strategy, Sahasra Semiconductors Pvt. Ltd.
7. Shri Rajendra Pratap, Vice President, Digital and Computing, VerveSemi Microelectronics Pvt. Ltd.

Outcome of the Workshop

The workshop on "Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities" resulted in a comprehensive and multi-dimensional understanding of India's semiconductor landscape and the strategic actions required to strengthen it.

A key outcome was the recognition of India's "semiconductor paradox"—strong capabilities in chip design but heavy dependence on imports for manufacturing and materials. Participants agreed that addressing this gap requires a balanced and integrated approach combining R&D, design, manufacturing, policy support, and skill development.

The discussions led to a consensus on the need for focused strategic interventions. These include promoting design-led innovation, developing pilot fabrication facilities, and encouraging indigenous materials and equipment manufacturing. The importance of investing in emerging domains such as AI chips, photonics, and sustainable electronics was also highlighted as a pathway for global competitiveness.

Another major outcome was the emphasis on workforce development. Participants stressed the urgent need to build a skilled, industry-ready talent pool through curriculum reform, structured training programs, and stronger academia-industry collaboration.

On the policy front, the workshop underscored the necessity of coherent governance frameworks and institutional strengthening. Recommendations included establishing a National Semiconductor Authority and a National Semiconductor Research Center, enhancing supply chain resilience, and promoting international partnerships and semiconductor diplomacy.

The workshop also identified critical challenges such as high capital intensity, technology access barriers, and weak commercialization pathways. Addressing these will require long-term policy stability, sustained investment, and coordinated stakeholder efforts.

Overall, the workshop concluded that semiconductors are a strategic imperative for India's economic growth, technological sovereignty, and national security, and achieving global competitiveness will depend on integrated, sustained, and mission-driven efforts across the ecosystem.

Key Challenges Identified

1. R&D and Innovation, Design, and Manufacturing Ecosystem

- High import dependency (≈95%) for semiconductors exposes India to major economic and strategic risks.
- Supply chain vulnerability highlighted during COVID-19, causing disruptions in sectors like automobiles.
- "India Semiconductor Paradox": strong global presence in chip design (~20% workforce) but weak domestic manufacturing capacity.
- Weak research-to-product translation, with most innovations ending at papers/patents rather than commercialization ("valley of death").
- Limited deep-tech entrepreneurship, as most startups focus on business models rather than IP-driven semiconductor innovation.
- Poor academia–industry–research collaboration, reducing effective knowledge transfer and industrial application.
- Insufficient R&D investment and patient capital needed for long-term semiconductor and deep-tech development
- Policy and institutional gaps, including lack of effective bridging mechanisms between academia, industry, and government
- Technology access constraints, with advanced nodes (<10nm) difficult due to high costs and limited global willingness to transfer technology
- Marginal presence across the semiconductor value chain, with heavy reliance on imports for equipment, materials, and manufacturing
- Lack of focus on niche, high-value, and strategically critical semiconductor domains
- Absence of pilot fabrication facilities, limiting transition from lab-scale research (TRL 3–4) to pilot-scale production (TRL 5–7)
- Missed opportunities in emerging domains such as wide bandgap semiconductors (GaN, SiC), photonics, and flexible electronics
- Manufacturing constraints, including high capital costs, limited access to advanced technology nodes, and risk of obsolescence.
- Limited commercialization of academic research, with gaps in IP generation, productization, and industry linkage
- Underdeveloped semiconductor manufacturing infrastructure, despite strong design talent and R&D presence

- Restricted access to cutting-edge technologies due to global market dynamics and geopolitical factors.
- Funding challenges, with lack of patient capital for long-term semiconductor and deep-tech development.
- Talent and curriculum gaps, including insufficient specialized training and industry-aligned education.
- Regulatory and procurement barriers, making it difficult for startups to secure initial customers and scale innovations.
- Low national R&D investment compared to global leaders, limiting innovation capacity and competitiveness.
- Commercialization challenges in sensors, including cross-sensitivity and reliability issues
- Need for long-term funding and patience, as semiconductor development cycles are slow and capital-intensive

2. Ecosystem for Skill Workforce & Talent Development

- Severe shortage of skilled workforce across the semiconductor value chain, including engineers, technicians, and infrastructure specialists.
- Severe shortage of skilled workforce, not only for fab operations but also for construction, cleanroom design, utilities, and maintenance
- Gap between academic training and industry requirements, with limited hands-on fabrication and cleanroom exposure
- Imbalance in talent supply, with strong design talent but shortage of fabrication engineers, ATMP specialists, and technicians
- Low awareness and accessibility of semiconductor education, especially among students from non-elite or remote backgrounds
- Fragmented skilling ecosystem, lacking coordination between training institutions, academia, and industry needs
- Dependence on foreign training and expertise, requiring sending talent abroad for advanced skills
- Weak integration of physics, manufacturing, and design knowledge, limiting IP creation and deep-tech innovation
- Inadequate infrastructure for training, including shortage of university-level cleanrooms and fabrication facilities
- Absence of specialized training tracks for sectors like aerospace and defense (e.g., radiation-hardened chips, certification standards)
- Narrow definition of semiconductor skills, overlooking ecosystem roles such as IP lawyers, finance experts, and technology managers
- Weak industry–academia collaboration in curriculum design, training, and research translation

- Challenges in scaling workforce training, given the rapid expansion of semiconductor projects across multiple states
- Shortage of professionals in IP law, venture finance, semiconductor economics, and business strategy.
- Low visibility of training institutions and programmes, restricting student participation.
- Weak outreach and engagement limit talent pipeline expansion.

3. Policy, Governance, and Institutional Framework

- Aerospace & defense constraints: Long lifecycle systems (30+ years) require stable, non-substitutable semiconductor components with assured long-term availability.
- Security risks: Threats from counterfeit chips, malicious code, and untrusted fabrication sources; FPGA vulnerabilities and reliance on foreign toolchains.
- Strict certification requirements: Absence of a domestic regulatory framework for aerospace-grade semiconductor validation (e.g., radiation-hardening, safety compliance).
- Lack of trusted domestic foundries for strategic sectors.
- Incomplete Indigenous Capability: Absence of end-to-end semiconductor ecosystem (design + fabrication + tools + testing).
- Dependency on foreign EDA tools, compilers, and software toolchains, even for "indigenous" designs.
- Limited control over IP and design rights, especially for long-term programmes.
- Weak Innovation-to-Commercialization Linkages: University–industry collaboration remains fragmented and poorly governed, and lack of institutional mechanisms to move technologies from TRL 3–4 to TRL 7–8.
- Limited control over IP and design rights, especially for long-term programmes
- Policy Fragmentation & Governance Gaps: Absence of a central coordinating authority for semiconductor R&D and policy execution, and Limited policy feedback mechanisms for iterative improvement of initiatives
- Policy and regulatory gaps: Lack of long-term stable policies, certification standards, and trusted domestic fabs for strategic sectors.
- India contributes significantly to chip design talent but owns limited IP.
- Limited technology readiness and manufacturing maturity.
- Aerospace, defence, and strategic sectors require specialized chips, standards, and secure supply chains not addressed by general semiconductor policy.
- Raw Material & Resource Constraints: Limited domestic reserves of critical minerals and rare earth element and heavy dependence on countries (especially China) for processing and supply chains.
- Low R&D Intensity: Insufficient investment in semiconductor R&D compared to global leaders

- Technology gaps: India lags behind global leaders (≥40nm vs <5nm nodes), requiring major investments and expertise.
- Slow cluster development: Semiconductor hubs are still emerging and lack ecosystem integration.
- Limited international collaboration: Insufficient partnerships for technology transfer and global integration.

4. Strategic Pathways: A Roadmap for India's Semiconductor Future

- Fragmented semiconductor ecosystem with strong design capabilities but weak presence in manufacturing, materials, and equipment ("missing middle").
- Strong in design and consumption, but limited presence in fabrication and supply chain.
- Limited access to physical fabrication training; need large-scale workforce development
- Lack of end-to-end integration across the semiconductor value chain.
- Uneven reach of advanced training across Tier 2 and Tier 3 cities.
- Limited fabrication training access, as high-cost cleanroom infrastructure restricts hands-on learning opportunities.
- Policy gaps in R&D integration, with earlier initiatives not fully incorporating research institutions into national missions.
- There are barriers to industry–lab collaboration, especially when technology originates domestically
- Lack of Full stack capability: India largely operates in fabless design, missing value from manufacturing and packaging.
- Semiconductor ecosystem requires multi-disciplinary expertise (mechanical, chemical, electrical, materials science); existing education system not fully aligned to produce industry-ready interdisciplinary talent at scale.
- Weak domestic supplier ecosystem, leading to heavy dependence on imports for chemicals, components, and equipment.
- Underutilization of intellectual property (IP) despite strong talent, resulting in low value capture.
- Barriers to adoption of indigenous products, as domestic firms face credibility challenges against global competitors.
- Restrictive global IP regimes, limiting technology access and industrial learning pathways.
- Lack of full-stack capability, with gaps across fabrication, packaging, testing, and product development.
- Insufficient coordination among national initiatives, reducing the overall effectiveness of semiconductor policies.

Recommendations

1. R&D and Innovation, Design, and Manufacturing Ecosystem

- Strengthen domestic manufacturing while prioritizing IP creation, ensuring India captures high-value segments of the semiconductor value chain
- Develop Semiconductor Translation Hubs to bridge the gap between academia (TRL 1–3) and industry-ready products (TRL 7–9)
- Increase R&D investment and enable patient capital, supporting long-term deep-tech innovation and semiconductor development
- Promote deep-tech startups and IP-driven unicorns, including a flagship "anchor" company to catalyze the ecosystem
- Adopt a diversified technology strategy, focusing on areas like sensors, power electronics (GaN/SiC), photonics, packaging, and automotive chips
- Adopt a niche-focused semiconductor strategy, prioritizing high-value, strategic segments such as compound semiconductors, RF devices, MEMS sensors, and defense applications
- Encourage development of domestic supplier ecosystems (materials, components, precision engineering)
- Utilize global opportunities like "China+1" to integrate into supply chains while building domestic capabilities
- Establish pilot fabrication facilities and shared national cleanrooms to bridge the gap between lab research (TRL 3–4) and pilot production (TRL 5–7).
- Strengthen coordination among research institutions to align efforts with national semiconductor priorities.
- Build an integrated ecosystem linking R&D, industry participation, and manufacturing capabilities.
- Promote strong academia–industry collaboration for technology validation, scaling, and commercialization.
- Expand academic infrastructure and semiconductor education, including cleanrooms, specialized courses, and hands-on training.
- Encourage industry-oriented curriculum, internships, and chip design projects (e.g., tape-outs).
- Invest in emerging research domains like flexible electronics, photonics, neuromorphic systems, and quantum technologies.
- Develop domestic capabilities in critical materials (e.g., gallium, GaAs, GaN, SiC) to reduce import dependence and supply risks

- Promote regional semiconductor clusters, each specializing in specific technologies to build depth and ecosystem efficiency
- Strengthen IP generation and commercialization pathways, including mandatory patenting for publicly funded research and industry linkages
- Create strong domestic demand signals through policy alignment across electronics manufacturing, system integration, and end-product markets
- Expand semiconductor infrastructure in academia, including cleanrooms, tape-out programs, and industry-oriented curriculum
- Invest in emerging technology areas such as photonics, quantum semiconductors, flexible and biodegradable electronics, and neuromorphic hardware
- Support domestic equipment manufacturing, including long-term funding for indigenous tool development (e.g., CVD reactors)
- Address advanced packaging and process gaps, including plasma-based technologies and MEMS fabrication challenges
- Promote sustainable and additive manufacturing approaches, including biodegradable and flexible electronics
- Support sensor commercialization efforts, including solving technical challenges like cross-sensitivity through collaborative R&D
- Include compound and wide bandgap semiconductors (GaN, SiC) as a dedicated focus area under ISM 2.0
- Enable long-term funding and policy stability, recognizing the capital-intensive and time-intensive nature of semiconductor development
- Improve procurement systems and maintenance infrastructure for sustained fab performance.
- Align semiconductor strategy with global supply chains rather than focusing only on import substitution.
- Integrate R&D investment, manufacturing incentives, and demand creation policies for holistic growth.
- Strengthen technology commercialization pathways to move innovations from labs to markets.
- Build resilient supply chains by reducing dependence on imports and diversifying sourcing.
- Support long-term innovation and infrastructure sustainability through coordinated national strategies.

2. Ecosystem for Skill Workforce & Talent Development

- Scale semiconductor workforce development at mission level, addressing both operational and construction-phase skill requirements (fabs, cleanrooms, utilities)

- Expand hands-on training infrastructure, including university cleanrooms, pilot facilities, and digital twin-based fabrication training platforms
- To include non-engineering roles such as technicians, cleanroom operators, and infrastructure specialists in skilling programmes.
- Develop a comprehensive workforce pipeline covering design, fabrication, packaging, testing, and system integration.
- Strengthen industry-aligned curriculum, integrating design, device physics, and manufacturing processes to build end-to-end competency
- Leverage virtual learning platforms (e.g., cloud-based EDA labs) to democratize access to chip design education across Tier 2/3 institutions
- Develop a tiered skilling pathway (Levels 0–3 and beyond), with domestic training followed by advanced international exposure
- Create specialized talent pipelines for fabrication engineers, ATMP specialists, and cleanroom technicians
- Introduce dedicated training verticals for strategic sectors like aerospace and defense (radiation-hardened chips, certification standards such as DO-254)
- Strengthen industry–academia partnerships, including co-designed courses, internships, joint research, and micro-credential programs
- Promote interdisciplinary skill development, including semiconductor economics, IP law, technology valuation, and venture financing
- Establish semiconductor skilling centers near fab clusters to ensure localized workforce availability
- Enhance accessibility and awareness, including entry-level courses for beginners and outreach to underserved regions
- Expand national semiconductor skilling infrastructure through Centers of Excellence, training platforms, and virtual labs.
- Strengthen industry partnerships to provide exposure to real-world design flows, fabrication, and packaging processes.
- Introduce interdisciplinary programmes combining semiconductors with AI, materials science, and electronics.
- Ensure long-term policy stability (10–15 years) to support infrastructure, investment, and workforce planning
- Encourage global talent attraction and reverse brain drain, bringing experienced semiconductor professionals to India
- Align skilling initiatives with national semiconductor projects, ensuring workforce supply matches project timelines and needs

- Promote collaborative use of infrastructure, such as shared cleanroom facilities across institutions to optimize costs and access
- Build India as a global semiconductor talent hub through a phased strategy:
  - Short term: strengthen design and ATMP capabilities
  - Medium term: expand fabrication and materials ecosystem
  - Long term: achieve balanced leadership in manufacturing, innovation, and IP development

3. Policy, Governance, and Institutional Framework

- 'National Semiconductor Authority' may be established to coordinate semiconductor policy, R&D programmes, industry participation, and long-term strategic planning, particularly for critical sectors such as aerospace, defense, and advanced digital technologies
- A specialized certification and regulatory framework may be introduced to ensure reliability, security, and performance semiconductors use in strategic sectors
- A centralized national verification and security mechanism may be established to validate chip integrity, detect vulnerabilities, and ensure compliance with aerospace and defense safety requirements
- Need to establish trusted domestic semiconductor foundries that meet strict security and reliability standards
- Need to create 'specialized certification standards' for aerospace-grade and defense-grade semiconductors
- Develop complete toolchains (design → compile → verification → testing) alongside chip fabrication
- Strengthen Innovation Ecosystem & Policy Coherence through innovation models like quadruple-helix systems (industry–academia–government–society)
- Develop clear governance structures for university–industry collaboration
- Establish an India Semiconductor Research Centre (similar to global models like NSTC) for coordinating and popularizing research in semiconductor field
- Focus on Strategic Niche Capabilities: Identify and invest in critical segments in the value chain (e.g., sensors, aerospace chips, specialized materials).
- Develop separate semiconductor strategies for strategic sectors (aerospace, defence, AI, telecom).
- Maintain stable semiconductor policies over 10–15 years to match industry lifecycle timelines
- Address Raw Material and Supply Chain Vulnerabilities and Integrate geopolitical risk assessment into semiconductor strategy
- Ensure IP ownership and long-term control over processors, FPGAs, and embedded systems.
- Expand and Deepen Design-Linked Incentives (DLI) to support IP-based chip design startups

- Accelerate AI Semiconductor Opportunities by supporting startups in AI-specific chip design (SoCs, edge AI processors), promoting FPGA-based and customized AI hardware **solutions**, and investing in AI-enabled packaging and cloud semiconductor infrastructure
- Promote development across low-, mid-, and high-end semiconductor segments for strategic sectors
- Develop Semiconductor Diplomacy & Global Integration to secure critical raw materials (rare earths, GaN, etc.)**.**
- Build bilateral and multilateral partnerships for technology transfer and supply chain integration.

4. Strategic Pathways: A Roadmap for India's Semiconductor Future

- Expand virtual semiconductor training platforms to scale education and reach Tier 2 and Tier 3 institutions.
- Build the "missing middle" by investing in manufacturing, materials, and semiconductor equipment ecosystems.
- Integrate R&D institutions into national semiconductor missions to strengthen innovation and technology translation.
- Build a full-stack semiconductor ecosystem (design → fabrication → packaging → testing → products)
- Strengthen industry–academia–lab collaboration through structured programmes and funding support
- Develop a robust domestic supplier ecosystem through incentives and industry–academia collaboration.
- Promote hands-on fabrication training programmes alongside simulation-based learning.
- Establish a national knowledge and IP economy framework to encourage innovation, IP creation, and monetization.
- Invest in interdisciplinary R&D and talent development across engineering domains
- Provide policy incentives and procurement support for adoption of indigenous semiconductor products.
- Encourage open innovation and learning-by-doing within legal and ethical IP boundaries.
- Ensure coordination across ISM, DLI, and broader policy frameworks to create a cohesive and self-reliant semiconductor ecosystem.

Way Forward

Moving forward, India's semiconductor development strategy should adopt a comprehensive and integrated approach that combines innovation, manufacturing capability, workforce development, and international collaboration. Building a resilient semiconductor ecosystem will require sustained policy support, long-term investment, and coordinated action across government, industry, and academia. Strengthening research infrastructure, expanding deep-technology entrepreneurship, and developing specialized manufacturing capabilities in strategic niches will allow India to gradually strengthen its position in the global semiconductor industry.

Simultaneously, efforts should focus on creating an enabling environment that supports innovation-driven enterprises, promotes intellectual property creation, and encourages technology commercialization. By aligning national research priorities with industrial needs and strengthening global partnerships, India can progressively build a competitive semiconductor ecosystem capable of supporting technological self-reliance, economic growth, and national strategic interests in the decades ahead.

Annexure 1. Program

Workshop on Strengthening India's Semiconductor Ecosystem: Policies, Challenges, and Opportunities

Date: 27.02.2026 (Friday)

Venue: CSIR-NIScPR, Pusa Campus, New Delhi

Time	Programme
Inaugural Session	
10: 00 AM-10:05 AM	Welcome address by **Dr. Geetha Vani Rayasam**, Director, CSIR-NIScPR, New Delhi
10:05 AM-10:10 AM	Setting the Context **Dr. Vipan Kumar,** Chief Scientist & Head Energy, Environment and Sustainability (EES) Division, CSIR-NIScPR
10:10 AM-10:40 AM	Address by the Chief Guest **Prof. V. Ramgopal Rao**, Vice-Chancellor, BITS Pilani & Ex-Officio Member, ES Manufacturing Committee
10:40 AM-10:45 AM	Vote of Thanks **Dr. Naresh Kumar**, Chief Scientist & Head Innovation, Entrepreneurship, and Diffusion Research (IED), CSIR-NIScPR
Session I: **R&D and Innovation, Design, and Manufacturing Ecosystem** **Chair: Dr. Rajesh K Sharma**, Former Distinguished Scientist and Director, Solid State Physics Laboratory, DRDO, Delhi, & Chairman, Semiconductor Society (India) **Co-Chair: Dr. Naresh Kumar**, Chief Scientist, CSIR-NIScPR, New Delhi	
10:45:00 AM – 12:30 PM	**Dr. Manish Mathew** Senior Principal Scientist & Head, Diamond Research Group (DRG) CSIR-CEERI, Pilani **Ms. Dipakshi Mehandru**, Director, Government Affairs, Intel India **Dr. Rahul Kumar** Associate Head, Center for Research Excellence in Semiconductor Technologies (CREST), BITS Pilani **Dr. Umesh Kumar Tiwari** Senior Principal Scientist & Head, Optics & Photonics Instrumentation (OPI), CSIR- CSIO, Chandigarh **Dr. Nirmalya Karar** Senior Principal Scientist, CSIR-NPL, New Delhi **Prof. Shree Prakash Tiwari** , Professor, Dept. of Electrical Engineering & Dean of Administration, IIT Jodhpur
Session II: **Ecosystem for Skill Workforce & Talent Development** **Chair: Dr. Manish K Hooda**, Director (Technology), India Semiconductor Mission, MeitY Govt. of India, New Delhi **Co-Chair: Dr. Bornali Sarma**, Senior Principal Scientist, CSIR-NIScPR, New Delhi	

<table>
<tr><td>12:30 PM – 1:30 PM</td><td>Dr. Ripunjay Singh,
Scientist-E, NIELIT, New Delhi

Prof. Awanish Pandey
Assistant Professor Dept. of Optics & Photonics Centre, & Programme Coordinator - Semiconductor Manufacturing and Technology, IIT-Delhi

Prof. Rishu Chaujar,
Director, Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Department of Applied Physics, DTU, New Delhi</td></tr>
<tr><td>01:30 PM - 02:30 PM</td><td>Lunch</td></tr>
<tr><td colspan="2" align="center">Session III: Policy, Governance, and Institutional Framework
Chair: Prof. Sujit Bhattacharya, Adjunct Professor, Amrita University, Former Chief Scientist, CSIR-NIScPR & Professor (AcSIR)
Co-Chair: Dr. Vipan Kumar, Chief Scientist & Head Energy Environment & Sustainability Division, CSIR-NIScPR, New Delhi</td></tr>
<tr><td>02:30 PM – 04:00 PM</td><td>Dr. C.M. Ananda
Chief Scientist & Head, Aerospace Electronics Division, CSIR-NAL, Bengaluru

Prof. Sujit Bhattacharya
Adjunct Professor, Amrita University, Former Chief Scientist, CSIR-NIScPR & Professor (AcSIR)

Dr. Shiv Narayan Nishad Principal Scientist, CSIR-NIScPR New Delhi
& Dr. Sandhiya L.
Senior Scientist, CSIR-NIScPR New Delhi
Ms. Naba Suroor,
Science & Technology / Atal Innovation Mission Division, NITI Aayog, Government of India, New Delhi
Dr. Amit Kumar,
Assistant Professor, Research and Information System for Developing Countries (RIS), New Delhi</td></tr>
<tr><td colspan="2" align="center">Panel Discussion and Concluding Session: Strategic Pathways: A Roadmap for India's Semiconductor Future
Chair: Prof. Navakanta Bhat, Dean, Division of Interdisciplinary Sciences, Professor, Centre for Nanoscience and Engineering, Indian Institute of Science (IISc), Bengaluru
Co-Chair: Dr. Sujit Bhattacharya, Adjunct Professor, Amrita University, Former Chief Scientist, CSIR-NIScPR & Professor (AcSIR)</td></tr>
<tr><td>4:00 PM – 5:30 PM</td><td>Dr. Roopa Hegde,
Lead Engineer, Semiverse Solutions, Lam Research
Dr. Hemang Shah
Senior Director, Government Affairs and Business Development, Applied Materials India, Bengaluru, Karnataka
Dr. Manish Mathew
Head, Semiconductor Diamond Research Group (DRG), CSIR-CEERI, Pilani
Dr. George Paul
Director, Govt. Relations & Corporate Strategy, Sahasra Semiconductors Private Limited, New Delhi
Shri Rajendra Pratap
Vice President (Digital & Computing), VerveSemi Microelectronics (P) Ltd, Noida, UP
Dr. Rahul Kumar , Associate Head, Center for Research Excellence in Semiconductor Technologies (CREST), BITS Pilani</td></tr>
<tr><td></td><td>Concluding Remarks
Dr. Vipan Kumar, Chief Scientist, CSIR-NIScPR
Dr. Charu Verma , Chief Scientist, CSIR-NIScPR</td></tr>
</table>

Annexure 2: List of Experts (Alphabetical Order)

S. No.	Name	Organization
1	Dr. Amit Kumar	Assistant Professor, Research and Information System for Developing Countries (RIS), New Delhi
2.	Prof. Awanish Pandey	Assistant Professor, Optics & Photonics Centre & Programme Coordinator, IIT Delhi
3.	Dr. Bornali Sharma	Senior Principal Scientist, CSIR-NIScPR, New Delhi
4.	Dr. C.M. Ananda	Chief Scientist & Head, Aerospace Electronics Division, CSIR-NAL, Bengaluru
5.	Ms. Dipakshi Mehandru	Director, Government Affairs, Intel India
6.	Dr. George Paul	Director, Govt. Relations & Corporate Strategy, Sahasra Semiconductors Pvt. Ltd., New Delhi
7.	Dr. Geetha Vani Rayasam	Director, CSIR-NIScPR, New Delhi
8.	Dr. Hemang Shah	Senior Director, Govt. Affairs & Business Development, Applied Materials India, Bengaluru
9.	Dr. Manish K Hooda	Director (Technology), India Semiconductor Mission, MeitY, New Delhi
10.	Dr. Manish Mathew	Senior Principal Scientist & Head, DRG, CSIR-CEERI, Pilani
11.	Ms. Naba Suroor	Science & Technology / Atal Innovation Mission Division, NITI Aayog, New Delhi
12.	Dr. Naresh Kumar	Chief Scientist, CSIR-NIScPR, New Delhi
13.	Prof. Navakanta Bhat	Dean, Division of Interdisciplinary Sciences, IISc Bengaluru
14.	Dr. Nirmalya Karar	Senior Principal Scientist, CSIR-NPL, New Delhi
15.	Prof. Rishu Chaujar	Director, Vinod Dham Centre of Excellence, DTU, New Delhi
16.	Dr. Rahul Kumar	Associate Head, CREST, BITS Pilani
17.	Dr. Rajesh K Sharma	Former Distinguished Scientist & Director, SSPL, DRDO; Chairman, Semiconductor Society (India)
18.	Shri Rajendra Pratap	Vice President, VerveSemi Microelectronics Pvt. Ltd., Noida
19.	Dr. Ripunjay Singh	Scientist-E, NIELIT, New Delhi
20.	Dr. Roopa Hegde	Lead Engineer, Semiverse Solutions, Lam Research
21.	Dr. Sandhiya L	Senior Scientist, CSIR-NIScPR, New Delhi
22.	Dr. Shiv Narayan Nishad	Principal Scientist, CSIR-NIScPR, New Delhi
23.	Prof. Shree Prakash Tiwari	Professor & Dean, IIT Jodhpur
24.	Prof. Sujit Bhattacharya	Adjunct Professor, Amrita University; Former Chief Scientist, CSIR-NIScPR
25.	Dr. Umesh Kumar Tiwari	Senior Principal Scientist & Head, OPI, CSIR-CSIO, Chandigarh
26.	Prof. V. Ramgopal Rao	Vice-Chancellor, BITS Pilani
27.	Dr. Vipan Kumar	Chief Scientist, CSIR-NIScPR, New Delhi


ABOUT US

CSIR-National Institute of Science Communication and Policy Research (NIScPR), New Delhi

CSIR-National Institute of Science Communication and Policy Research (CSIR-NIScPR) is a constituent laboratory of Council of Scientific and Industrial Research carrying a broad mandate to promote STI policy studies and science communication among diverse stakeholders and act as a bridge at the interface of science, technology, industry, and society, which is essential to a robust S&T ecosystem in the country. The institute draws from the rich intellectual diversity of faculty in policy research and science communication. The core research activity of the institute is in different areas of the STI ecosystem, developmental challenges identified under sustainable development goals, and science-society studies with strong alignment to government policy and programs. Evidence-based policy research, socio- economic impact assessment, and outreach to society through diverse communication interactions are the focal approaches of the research. The institute also has 15 journals in different areas of science and technology, along with publishing a popular science magazine, Science Reporter, and R&D newsletters.

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